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REQUIREMENT SPECIFICATION

SS7 Communication Controller Board for PMC

Abstract: This requirement specification will be used as input when designing the SS7-PMC board. It is the output of the feasibility phase.

Template Data

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Prepared: EIN/R/C Tim Petterson, *Approved:* EIN/I/D (T. Nordholm)

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Enclosures

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1 Introduction

1.1 Revision History

Table 1: Revision History

Rev	Date	Prepared	Comment
A	1999-04-30	EINJOSK	First release from the prestudy. Old document number. Input document to the feasibility phase.
A	1999-10-28	EINJOSK	Updated during feasibility phase. Document number changed from 850012-02:02 to 1056-ROA 209 21/1 Uen. PN3 removed from (Figure 2). The switch and the LEDs are moved. RS1: Recommendation of FPGA type is removed. RS3: Loading through serial adapter is not essential. RS43: LED in the front is made optional. RS66 and RS67: Both 3,3 and 5V signalling levels should be supported. RS69: PRSNT pins are not used.
B	2000-09-12	EINJOSK	Updated verification method where it was TBD. Changed instance on prepared and approved.

1.2 General

1.2.1 Purpose

This document is created as an input to the design of a PMC communication controller board for SS7. This activity is part of a feasibility study for an SS7 communication controller board for PMC. Today a board with similar functions is being developed at EIN.

The board under development is a PCI board for desktop computers. The MTP2 protocol is implemented in an FPGA.

It is the intention that the PMC board will use the same FPGA MTP2-solution as for the PCI board.

1.3 Completeness

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1.4 Terminology

1.4.1 Acronyms

CMC	Common Mezzanine Card
CPCI	Compact PCI
CT bus	Computer Telephony bus
E1	2.048 Mbit/sec compliant to ITU G.703.
ECTF	Enterprise Computer Telephony Forum (H.110 standard)
EMC	Electro-Magnetic Compatibility
FPGA	Field Programmable Gate Array.
HCL	Hardware Compatibility List. Microsoft.
JTAG	IEEE 1149.1 boundary scan.
LED	Light Emitting Diode
MTBF	Mean Time Between Failures.
MTP2	Message Transfer Part layer 2. OSI link layer.
NDIS	Network Device Interface Specification.
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect.
PCM	Pulse Code Modulation.
PICMG	PCI Industrial Computer Manufacturers Group
PLD	Programable Logic Device
PM	Product Manager
PMC	PCI Mezzanine Card
SS7	Signal System no. 7
SS7-CPCI	SS7 Communication Controller Board for CompactPCI
SS7-PCI	SS7 Communication Controller Board for PCI
SS7-PMC	SS7 Communication Controller Board for PMC
T1	1.548 Mbit/sec compliant to ITU G.703.
TDM	Time Division Multiplex
TTE	Tele Terminal Equipment
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit.

1.4.2 Glossary

Requirement Priority: Conditional

Implies that these are requirements that would enhance the system, but not would make them unacceptable if they are absent.

Requirement Priority: Essential

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Implies that the system will not be acceptable unless these requirements are provided.

Requirement Priority: Optional

Implies a class of functions that may or may not be worthwhile.

1.5 References

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- ref. 1 155 19-CNA 107 378/1 Uen
MTP2 register model. An interface described in VHDL. IWD for SS7-PCI MTPL2
- ref. 2 2/1056-CRA 119 39 Requirement Specification for E1N Portable SS7, SS7 Communication Controller Board (SS7-PCI)
- ref. 3 850012-02:01 List of Requirements, SS7-PMC

ANSI, ITU, TTC and Chinese Standard rec.

- ref. 4 ITU-G.703 Physical/electrical characteristics of hierarchical digital interfaces.
- ref. 5 ITU-G.704 Synchronous frame structures used at 1544, 6312, 2048, 8488 and 44 736kbit/s hierarchical levels.
- ref. 6 ITU-G.706 Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704.
- ref. 7 ITU-G.823 The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.
- ref. 8 ITU-I.431 Primary rate user-network interface - Layer 1 specification.
- ref. 9 ANSI-T1.403 Network-to-Customer Installation - DS1 metallic interface.
- ref. 10 GF001-9001 Technical Specification of SS7 for National Telephone of China.
- ref. 11 JT/G703 TTC standard for T1 (Japan)
- ref. 12 JT/I-431-a TTC standard for T1 (Japan)

Regulatory safety, EMC, Telecom, environment and customer standard rec.

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ref. 13	IEC60950	Second edition. Safety of information technology equipment, including electrical business equipment, international.
ref. 14	EN60 950:1992	Safety of information technology equipment, including electrical business equipment, Europe. Including amendments No. 1 to 4
ref. 15	UL1950	3rd edition. Safety of information technology equipment, including electrical business equipment, North America.
ref. 16	CAN/CSA C22.2 No. 950-95	Safety of information technology equipment, including electrical business equipment, North America.
ref. 17	ETS300386-1	Public telecommunication network equipment Electro-Magnetic Compatibility requirements, Europe.
ref. 18	ETS300019-1-3	Environmental conditions and environmental tests for telecommunications equipment. Classification of environmental conditions. Stationary use at weather protected locations.
ref. 19	CISPR 22	Limits and methods of measurement of radio interference characteristics of information technology equipment, international.
ref. 20	FCC part 15	Federal Communications Commission. Radio frequency devices, North America.
ref. 21	FCC part 68	Connection of Customer-Provided Terminal Equipment to the Telephone Network.
ref. 22	PICMG 2.0 R2.1	CompactPCI Specification, 1997-09-02
ref. 23	PICMG 2.5 R1.0	Computer Telephony on CompactPCI, 1998-04-03
ref. 24	PICMG 2.1 R1.0	CompactPCI, Hot Swap Specification 1998-08-03
ref. 25	IEEE P1386.1	Physical and Environmental Layers for PCI Mezzanine Cards, Draft 2.0 1995-04-04
ref. 26	IEEE P1386	Common Mezzanine Card Family, Draft 2.0 1995-04-04
ref. 27	H.110	H.110 Hardware Compatibility Specification: CT Bus, revision 1.0
ref. 28	ANSI/VITA 6.1	J2/P2 pinout for SC bus on VME (1996)

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- ref. 29 BR 4/1056-117 Uen
BR Global Requirement Specification of EMC
- ref. 30 91/263/EEC Tele Terminal Equipment Directive
- ref. 31 ANSI/VITA 6 SCSA 1994; SC bus standard

2 Scope

This document is used as input for the design of the SS7-PMC, SS7 Communication Controller for PMC.

The main task of the SS7-PMC board is to execute the MTP2-layer protocol.

The SS7-PMC board is to be used in PMC computer systems to serve in applications such as intelligent nodes and gateways to telecom systems etc. It provides 4 E1/T1 interfaces which can be set up to run at 1.544 Mbit/sek or 2.048 Mbit/s. In addition to the PCI interface and the E1/T1 interfaces, the board is also equipped with a cascading interface over which several SS7-PMC boards can communicate.

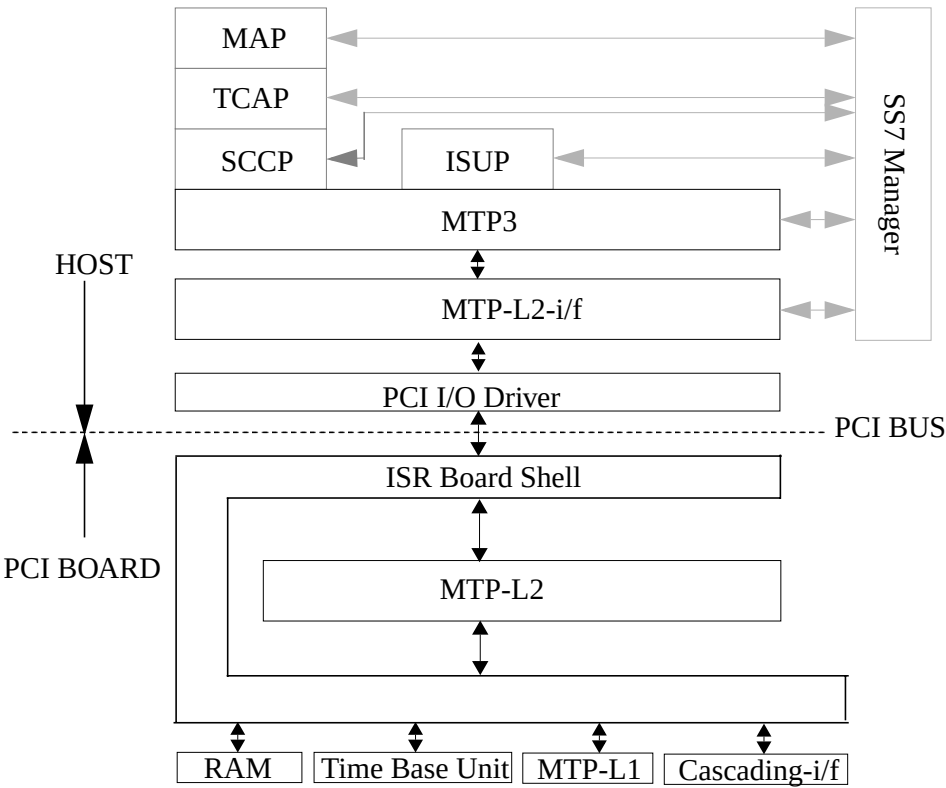


Figure 1 SS7 Architecture and ISR Environment on SS7-PCI

3 Functional Requirements

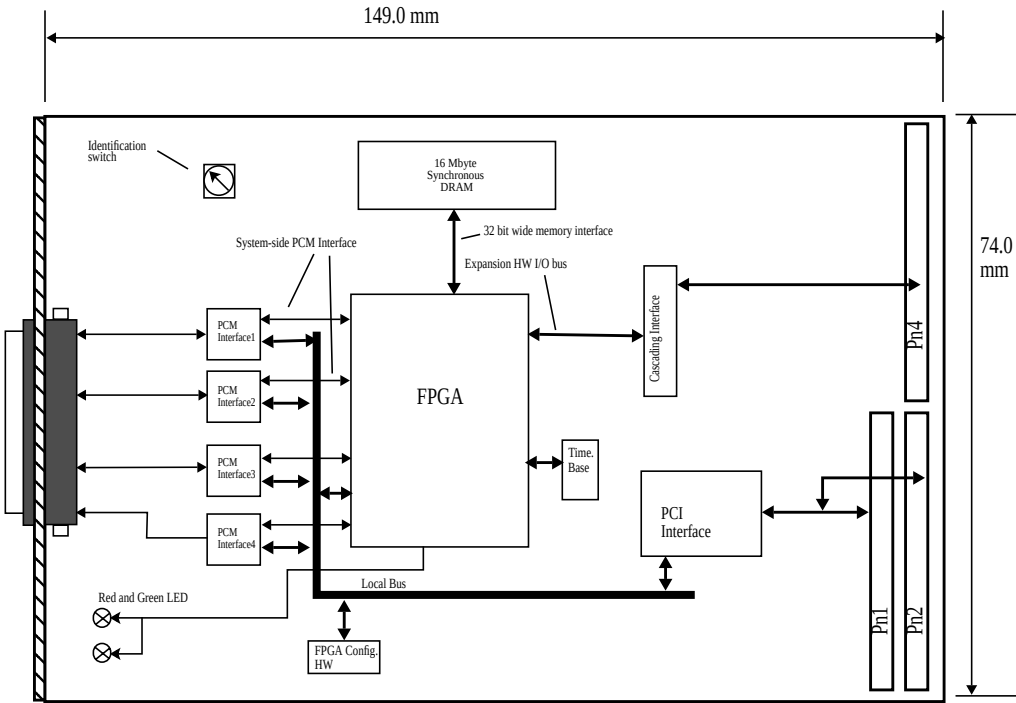


Figure 2 Functional Overview

3.1 FPGA

RS1:	Type of FPGA
	The board shall contain an FPGA corresponding to at least 300K gates.
Source:	EINJOSK
Verification:	Inspection
Priority:	Essential

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RS2: Package

The FPGA shall have a future safe package, so that future higher density FPGAs can be mounted on the same footprint. Proposed implementation: BGA 432.

Source: [ref. 2] (~~RS16~~)

Verification: Inspection

Priority: Essential

3.1.1 FPGA Configuration Hardware**RS3: Configuration Sources**

It shall be possible to load the FPGA application over the PCI interface.

Source: [ref. 2] (~~RS17~~)

Verification: Test with SS7 system

Priority: Essential

RS4: Application Load Indication

It shall be possible to read a status register from the host that indicates if the application was successfully loaded or not.

Source: [ref. 2] (~~RS19~~)

Verification: Test with SS7 system

Priority: Essential

3.2 PCI Interface

RS5: Level of Operation

The PCI interface shall have both target and initiator capability.

Proposed implementation: PLX Technology PCI9054.

Source: [ref. 2] (~~RS20~~)/ Omicron

Verification: According to [RS73:]

Priority: Essential

Comment: It is desired that the board will be able to handle hot swap when it is mounted on a CompactPCI board that supports hot swap. However, the cost and feasibility of hot swap needs to be further investigated.

RS5.1: Hang Proof

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The PCI interface must be hang-proof. If one board ceases to function it must still be possible to address other boards on the PCI bus.

Source: PM SS7

Verification: According to [RS73:]

Priority: Essential

3.3 PCM Interface

REQ1: Number of PCM Interfaces

The board shall have 4 physical PCM interfaces.

Source: PM-SS7

Verification: Inspection

Priority: Essential

RS6: Applicable Standards

The physical interface shall comply to ITU-G.703, ITU-G.704, ITU-G.706, ITU-G.823, ITU-I.431, and ANSI-T1.403.

Proposed implementation: Siemens PEB22554 (QuadFALC)

Source: [ref. 2] (~~RS21~~)

Verification: According to [RS74:]

Priority: Essential

Comment: If the QuadFALC is used it will be impossible to choose PCM standard per physical PCM interface.

RS7: Termination

E1 75/120 Ohm and T1 100 Ohm termination. Selection is adaptation cable dependent.

Proposed implementation: Termination is software controlled.

Source: [ref. 2] (~~RS22~~)

Verification: Design verification PCB

Priority: Essential

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RS8: Control of Transmission Parameters

All transmission parameters shall be software controlled (no jumpers).

Source: [ref. 2] (~~RS23~~)

Verification: Inspection

Priority: Essential

RS9: Independence Between Interfaces

Removed.

RS10: Interrupts

Interrupt request pins from the QuadFALC shall be routed to the FPGA.

Source: [ref. 2] (~~RS25~~)

Verification: Inspection

Priority: Essential

RS11: System-side PCM Interface

The system side PCM interface (between the PCM interface and FPGA) shall run at 2Mbit/s both for E1 and T1. The data clock shall be set up by the application and come from the time base unit.

Source: [ref. 2] (~~RS26~~)

Verification: Inspection

Priority: Essential

3.3.1 Interface Connectors**RS12: Generic PCM Interface Connectors**

Removed.

RS13: Regulatory Requirements

North America: FCC Part 68 and CS 03.

Source: [ref. 2] (~~RS28~~)

Verification: Inspection of connector specifications

Priority: Essential

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3.3.2 Short Adaptation Cable

RS14: PCM Interface Type Dependent Adaptor

The requirement is replaced by [REQ3:].

3.4 MPT1

RS15: Signalling Data Links

64 PCM timeslots shall be used for signalling data links in the nodes.

Source: EINJOSK

Verification: Design verification FPGA

Priority: Essential

RS16: Timeslot Allocation

Any timeslot except timeslot 0 for E1 shall be selectable as a signalling link.

Source: ERV

Verification: Design verification FPGA

Priority: Essential

RS17: Timeslot Availability

Removed.

RS18: PCM Systems

The requirement is removed.

RS19: Japan

Support for the 2 Japanese flavours of T1, JT/I-431-a and JT/G703, is desired.

Source: ERV

Verification: Design verification PCB

Priority: Conditional

Comment: The QuadFALC support these standards.

Japan uses other line-termination impedances than ITU/AN-SI.

RS20: ITU-T Standard Compliance

The MPT1 layer shall comply with Q.701-Q.703 ITU-T 1992.

Source: ERV

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Verification: Design verification PCB

Priority: Essential

RS21: ITU-T Blue Book Standard Compliance

Removed.

RS22: ANSI Standard Compliance

The MTP1 layer shall comply with T1.111 ANSI 1996.

Source: ERV

Verification: Design verification PCB

Priority: Essential

RS23: Standard Configuration

Removed.

RS24: Channelization

Removed.

3.5 MTP2

RS25: ITU-T Standard Compliance

Removed.

RS26: ANSI Standard Compliance

Removed.

RS27: Chinese Standard Compliance

Removed.

RS28: Japanese Standard Compliance

Removed.

RS29: Standard Configuration

Removed.

RS30: Error Correction

Removed.

RS31: Flow Control

Removed.

RS32: Alignment Procedure

Removed.

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RS33: Processor Outage
Removed.

3.6 RAM

RS34: 16 Mbyte RAM
The board shall be equipped with 16Mbyte RAM 32 bit wide.
Proposed implementation: A 16Mbyte 32 bit wide synchronous DRAM bank with speed 15ns/66 MHz.
Source: [ref. 2] (~~RS31~~)
Verification: Inspection
Priority: Essential

3.7 Time Base Unit

RS35: PCM Interface shall be used as Reference
The time base unit shall lock on the 2.048 MHz bit rate extracted from one of the incoming PCMs or generated in one of the PCM interfaces. It may also lock on the cascading interface bit clock.
Source: [ref. 2] (~~RS32~~)/ERV
Verification: According to [RS75:]
Priority: Essential
Comment: Externally the PCM interface can be either 2.048 MHz or 1.544 MHz. Internally on the SS7-PMC board 2.048 MHz is used.

RS36: Generate own PCM clock
It shall be possible to generate an own rx/tx-clock.
Source: ERV
Verification: Design verification PCB
Priority: Essential

RS37: 8kHz pins
There shall be 2 user I/O pins for 8 kHz clocks. Clock in/out from/to.
Source: ERV
Verification: Design verification PCB
Priority: Essential

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RS38: Frequency

The time base unit shall run at a nominal frequency of 65.536 MHz. With no lock reference the “free running” interval shall be within +- 32 ppm from the nominal frequency.

Source: [ref. 2] ~~(RS33)~~

Verification: According to [RS75:]

Priority: Essential

RS39: Change of Reference Source

The time base unit shall allow change of bit rate clock reference source (PCM1 to PCM2, PCM3 to PCM4 etc.) without bit errors on any of PCM interfaces (or the remaining upon error on the master PCM interface). It is assumed that all four PCM interfaces have the same clock source somewhere higher up in the PCM hierarchy, so that the PCM interfaces just differ in phase. It is also assumed that loss of sync detected to alternative reference is connected is less than 10 seconds (application delay).

Source: [ref. 2] ~~RS34~~

Verification: According to [RS75:]

Priority: Essential

RS40: No Reference at Power up

The time base unit shall run at power up without lock signal.

Source: [ref. 2] ~~(RS35)~~

Verification: According to [RS75:]

Priority: Essential

RS41: Jitter Attenuation

The time base unit may not introduce jitter to such extent that the jitter requirement stated for the PCM interfaces becomes impossible to achieve. This requirement has importance when a clock slaved PCM interface distributes a clock reference to a master interface.

Source: [ref. 2] ~~(RS36)~~

Verification: According to [RS75:]

Priority: Essential

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3.8 Cascading Interface

RS42: CT-Bus Connector

An SC bus shall be implemented on the Pn4 connector according to [ref. 28] and [ref. 31]. Adjacent boards shall be able to communicate across the backplane. Mechanically and electrically compliant to SC bus.

SC bus is a sub set of the H.100 standard.

Source: [ref. 2] (~~RS37~~)/EINJOSK

Verification: Design verification FPGA

Priority: Essential

Comment: The PCI-SS7 board will be able to switch timeslots from 8 of 32 frames in the H.100 interface. Multiplexing all 32 frames with 128 timeslots will require so much capacity that it will not be possible to implement the MTP2 protocol in the FPGA.

3.9 Red and Green LED

RS43: LEDs

One red and one green LED. The LEDs shall be controlled from the application in the FPGA.

Source: [ref. 2] (~~RS39~~)

Verification: Design verification PCB

Priority: Optional

3.10 JTAG Interface

RS44: Test Interface

Devices supporting JTAG boundary scan chains shall be connected to form a scan chain for the complete board ending in a test connector.

Source: [ref. 2] (~~RS40~~)

Verification: Design verification PCB

Priority: Essential

3.11 Test Application

These requirements are removed since they are a concern of the host-application and FPGA-application but not a concern of the SS7-PMC board itself.

RS44.1: Board and Host Test Application

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Removed.

RS44.2: Memory test

Removed.

RS44.3: PCM Interface Test

Removed.

RS44.4: Timing Unit Test

Removed.

3.12 Identification

RS45: Electronic ID

Each board shall contain a read only electronic ID telling what version number the connected board has. It must be possible to identify the product number and the product revision through the electronic ID:

Source: [ref. 2] (~~RS66~~)

Verification: Design verification PCB

Priority: Essential

REQ2: Geographic Address

It must be possible to identify the board from the application.

Implementation proposal

(1) Board identification shall be implemented as on the SS7-PCI board.

Source: EINJOSK

Verification: Test in system environment.

Priority: Essential

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4 External Interface Requirements

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5 Performance Requirements

RS46: SS7 Signalling Links

The board shall be able to handle 62 signalling links at 1 Erlang per link and in full duplex.

Source: PM SS7

Verification: Test in SS7 environment

Priority: Essential

RS47: SS7 Signalling Links ERV

Removed.

RS48: ITU Standard Performance

Removed.

RS49: ITU Standard Performance

Removed.

5.1 Destinations and Routing

RS50: Destinations and Routing

RS50.1: Destination Definition

Removed.

RS50.2: Routes

Removed.

RS50.3: Signalling Links

Removed.

RS50.4: Signalling Link Sets

Removed.

RS50.5: Adjacent Signalling Point

Removed.

RS50.6: Signalling Links per Set

Removed.

RS50.7: Configurable Limits

Removed.

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6 Other Requirements

6.1 Maintenance and Support

6.2 Upgrading and Downgrading

6.3 Installation and Deinstallation

6.4 Reliability and Availability

6.5 Platforms and Compatibility

RS51: Backwards Compatibility

There must be no impact on the Layer 2 interface in the SS7 software.

Source: PM SS7

Verification: Test in SS7 environment

Priority: Optional

Comment: This applies for the operating systems that are supported today. Layer 2 will be affected by the choice of PCM interface circuits and PCI interface circuit.

RS52: MTPL2 Design

The Layer2 design must be identical with the SS7-PCI board.

Source: PM SS7

Verification: Inspection

Priority: Optional

Comment: If 4 E1/T1 interfaces are to be implemented the multiplexer function inside the FPGA application will be affected.

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6.6 Configuration, Changeability, Adaptability and Portability

6.7 Expansion and Flexibility

6.8 Human Engineering

6.9 Documentation and Training

6.10 Security

6.11 Safety

Safety of information technology equipment, including electrical business equipment.

RS53: International

Statement Of Conformity for IEC 60 950 second edition incl. Amendments No. 1 to 4.

Source: [ref. 2] (~~RS1~~)

Verification: Consulting SEMKO

Priority: Essential

RS54: Europe

Statement Of Conformity for EN 609 50:1992 incl. Amendments No. 1 to 4.

Source: [ref. 2] (~~RS2~~)

Verification: Consulting SEMKO

Priority: Essential

RS55: North America

ETL recognition.

Source: [ref. 2] (~~RS3~~)

Verification: Consulting SEMKO

Priority: Essential

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6.12 Computer Resources Reserve Capacity

6.13 Components

6.14 Transportability

6.15 Supply

6.16 Mechanical

RS56: PMC

Single size CMC shall be used. Mechanical construction shall comply with [ref. 26].

Source: ERV/EINJOSK

Verification: Design verification PCB

Priority: Essential

RS57: E1/T1 Connector Positioning

Removed.

RS58: E1/T1 Connector Grounding

The E1/T1 connectors shall be grounded to the front panel.

Source: ERV

Verification: Inspection

Priority: Essential

Comment: This is necessary to fulfil EMC requirements.

6.17 Environmental

6.17.1 EMC**RS59: International**

CISPR 22 Class B.

Source: [ref. 2] (~~RS4~~)

Verification: Consulting SEMKO

Priority: Essential

RS60: Ericsson GPRS

Design must be EMC aware, according to core requirements.

Source: ERV

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Verification: Consult ERV during the design phase

Priority: Essential

Comment: The GPRS platform (Core) has been testing various PMC modules. None of them has been satisfactory regarding EMC. There are some documents stating requirements on purchased PMC modules for GPRS. There are also test reports from experienced EMC problems particularly with the front panel I/O cables. ERV wants that their experiences are considered in the SS7-PMC design.

RS61: Europe

ETS 300386-1.

Source: [ref. 2] (~~RS5~~)

Verification: Consulting SEMKO

Priority: Essential

RS62: North America

FCC part 15.

Source: [ref. 2] (~~RS6~~)

Verification: Consulting SEMKO

Priority: Essential

RS63: BR EMC Requirements

The design must fulfil the requirements stated in the Ericsson internal document BR 4/1056-117 Uen ([ref. 29]).

Source: ERV

Verification: Consulting SEMKO

Priority: Optional

Comment: These requirements are wider than those in the EU directive ([ref. 17]). The class B requirements must be fulfilled. The BR requirements includes additional requirements believed to be added to the EU directive in the future. The EMC requirements are intended to make the product possible to sell worldwide.

6.17.2 Climate

Environmental conditions and environmental tests for telecom equipment.

RS64: ETSI

ETS 300019-1-3 with 48 h cycling at 40 degrees centigrade maximum temperature.

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Source: [ref. 2] (~~RS7~~)

Verification: Consulting SEMKO

Priority: Essential

RS65: Temperature

Temperature environment: 0-60 degrees centigrade. These limits refer to the temperature surrounding the PMC board.

Source: ERV

Verification: Consulting SEMKO

Priority: Essential

6.17.3 Characteristics

RS66: PCI compliance

The board shall comply with PCI v2.2, 5V and 3.3 V signalling, 32 bit, 33 MHz.

Source: PM SS7

Verification: Design verification PCB

Priority: Essential

RS67: PMC compliance

The board shall comply with [ref. 25]. Both 5V and 3.3V signalling shall be supported.

Source: PM SS7

Verification: Design verification PCB

Priority: Essential

RS68: Europe Tele Terminal

The SS7-PMC board must conform to the EU Teleterminal directive (TTE, [ref. 30]).

Source: ERV

Verification: Consulting SEMKO

Priority: Conditional

Comment: The TTE directive applies for equipment that are to be connected to the public network. It does not apply to equipment that is part of the network. It defines requirements for signal quality etc. It also states that the equipment shall be EMC compliant.

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RS69: Power dissipation

Maximum power dissipation shall comply with what is stated in [ref. 26] for single size CMC boards.

Source: [ref. 2] (~~RS10~~)/EINJOSK

Verification: Measurements

Priority: Essential

Comment: The board must be designed so that the power consumption can be measured.

RS70: MTBF

Removed.

RS71: Reset

It shall be possible to independently reset the

(1) PCM interface to an initial known state.

(2) FPGA to a ready to load application from host state.

Source: [ref. 2] (~~RS12~~)

Verification: Design verification PCB and PLD

Priority: Essential

RS72: Microsoft HCL

Removed.

6.18 Testing**RS73: PCI Interface Test**

A documented compliance test of PCI bus transaction protocol for both master and target termination shall be provided.

Source: [ref. 2] (~~RS67~~)

Verification: Inspection

Priority: Essential

RS74: PCM Interface Test

A documented compliance test verifying the PCM interface according to requirement [RS6:] shall be provided.

Source: [ref. 2] (~~RS68~~)

Verification: Inspection

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Priority: Essential

RS75: Time Base Unit and Memory Test

A documented test verifying the requirements for these units shall be provided.

Source: [ref. 2] (~~RS69~~)

Verification: Inspection

Priority: Essential

6.19 Delivery Packaging

RS76: Labelling

The board shall have an Ericsson product number and serial number label. This information shall be presented in plain text and in bar-code on the label.

Source: [ref. 2] (~~RS70~~)

Verification: Inspection

Priority: Essential

REQ3: PCM Interface Type Dependent Adaptor

An adaptor/adaptation-cable that adapts the various PCM standard connector types (E1 75/120 and T1 100) to the generic interface connector.

Source: [ref. 2] (~~RS30~~)/EINJOSK

Verification: Inspection

Priority: Essential

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7 Design Constraints

8 Requirement Verification Matrix

9 Precedence
