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DESIGN SPECIFICATION PCB

Abstract

The purpose of this design specification is to describe the *SS7 Communication Controller Board for PMC* (the SS7-PMC printed circuit board). The SS7-PMC board is based on the *EIN Portable SS7 Protocol Execution PCI Board* (the SS7-PCI board) [18]. The main differences is the physical format of the boards and that the SS7-PMC board has four channels instead of two. The design specification will serve as the basis for the design and implementation phase. For information about VHDL implementation in the PLD and the FPGA, see [3, 4, 5, 6, 7].

Revision History

Revision	Date	Author	Comment
A	000125	Magnus Eriksson	First Approved Version
PB1	000209	Magnus Eriksson	8kHz from PLD to FPGA removed 16.384MHz from PLD to FPGA removed
PB2	000803	Magnus Eriksson	Added 2.048MHz clock in timebase figure. Changed JTAG interface.
B	000807	Magnus Eriksson	Second Version

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GENERAL

In this design specification, "FPGA Application" means the software in the FPGA that is delivered by EIN. "Host" is the computer that the card is inserted in. "Host application" means the application that runs on the host computer.

The SS7-PMC printed circuit board is based on the PCI mezzanine card specification [19] and has the physical format of 149X74mm. The PMC specification is an add on to the CMC specification [17]. The board has a number of interfaces: one SCbus connector (the cascading interface), two PCI connectors and four PCM channels. The SCbus is a standard [15] that makes it possible for multivendor components to communicate within a standard PC. The board will support the 32 bit PCI bus [16].

The board will utilize a QuadFALC for handling the four PCM channels, a PCI controller, two SDRAMs, a PLD and an FPGA, making the board configurable.

The SS7-PMC board is based on the the SS7-PCI board, also developed for Ericsson Infotech in Karlstad.

[1] and [2] will act as a basis for this design specification.

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2 SCHEMATIC

2.1 BLOCK DIAGRAM

Fig.1. is a block diagram of the board. All blocks and interfaces in the diagram are described in detail later in this design specification. Note that a number of clocks are distributed in the system. These are described in chapter 6.

Fig.1. Block sketch.

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MEMORY MAP

Fig.2. describes the memory mapping that is made in the BAR registers in the PCI 9054 chip [10].

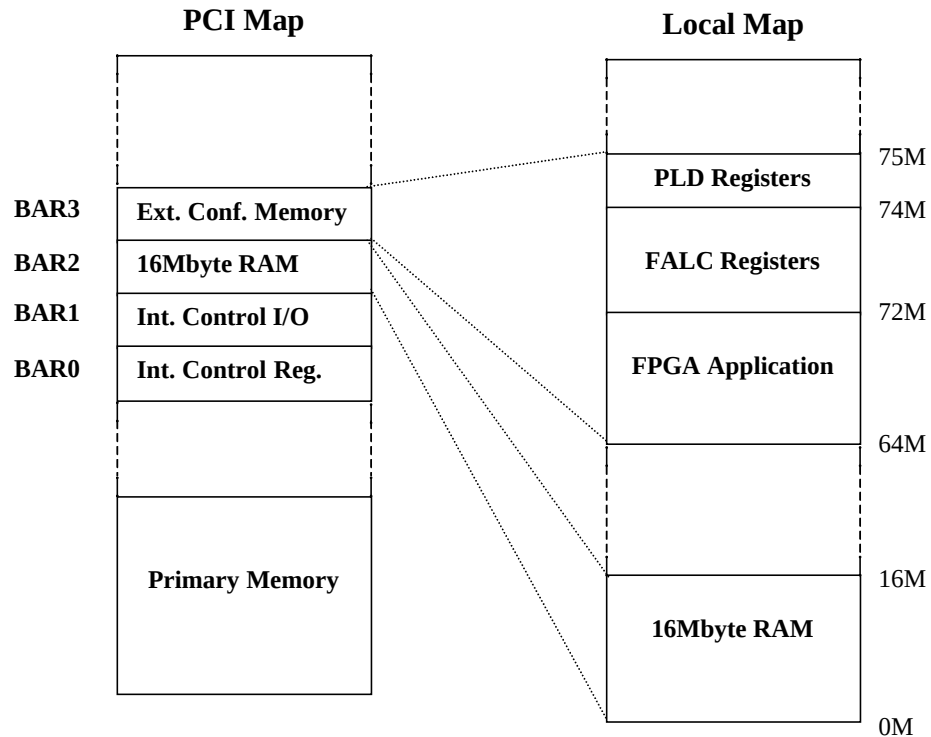


Fig.2. Board memory map

Four BAR registers are used.

- BAR 0: Internal Control Register
- BAR 1: Internal Control I/O
- BAR 2: 16Mbyte RAM
- BAR 3: External Configuration Registers

The external configuration memory is divided into four sub areas in the local map. Each sub area is between 1 and 8 Mbyte¹ large and contains several registers. The size and location of the memory areas is chosen so that the memory decoding can be kept simple. These registers are handled by an address decoder implemented in the FPGA.

(1)

1 Mbyte = 1024² bytes

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3.1 PLD MEMORY MAP

Four eight bit wide registers are used in the 1 Mbyte large PLD memory map. Fig.3. shows the memory map for the PLD area. The PLD Memory Map has an address offset of 74 Mbyte (04A00000h). The four registers are described in [3].

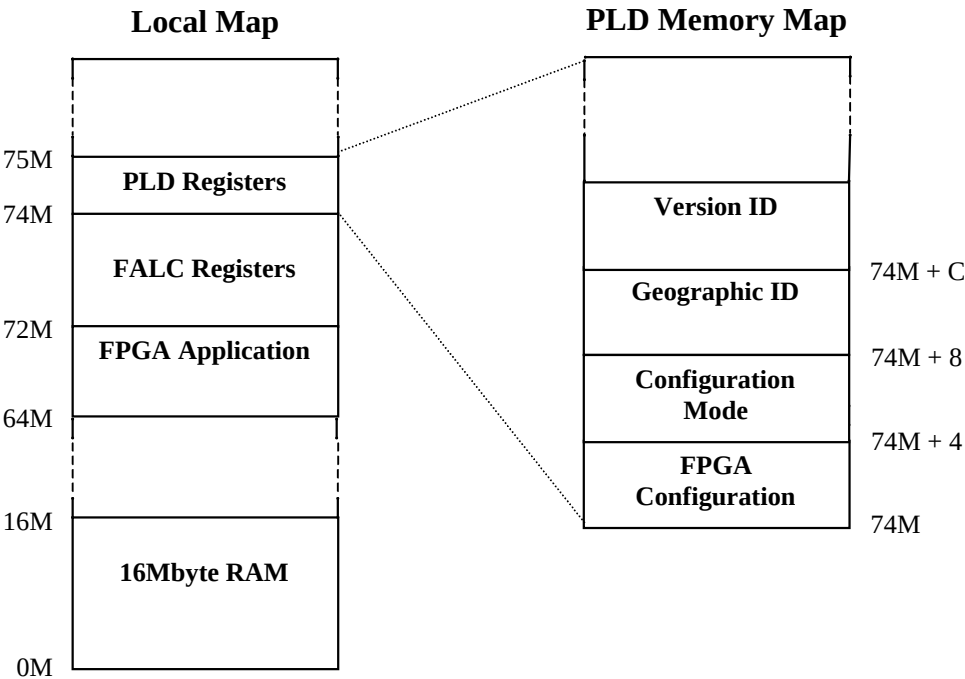


Fig.3. PLD memory map.

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3.2 QUADFALC MEMORY MAP

Fig.4. shows the memory map for the QuadFALC area. The QuadFALC Memory Map has an address offset of 72 Mbyte (04800000h).

Since the QuadFALC component operates in 8 bit data bus mode and the local bus is 32 bits wide, two things must be considered when performing a read or a write to the QuadFALC registers:

- 1 Only byte accesses can be made to the QuadFALC configuration registers. The 8 LSBs of the data bus will carry the data.
- 2 The QuadFALC register address offset, as specified in [9], must be multiplied by four in the host address for a proper translation because the local bus is 32 bits wide (can be configured for a width of 8 or 16 bits). Thus, the local address bus is mapped to the QuadFalc address bus as LA2->A0, LA3->A1,..., LA11->A9.

For example, if a read should be made from QuadFALC address 05h (Receive Address High 2) then a byte read access at address $5h * 4 = 14h$ should be made at the host application.

This is no different from the SS7-PCI board.

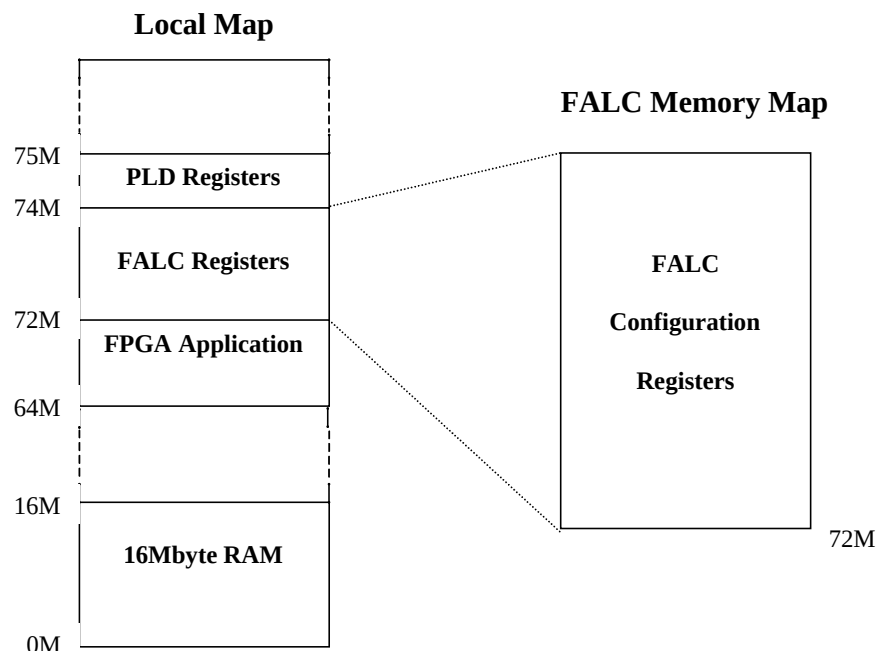


Fig.4. QuadFALC memory map

The QuadFALC Configuration registers are described in detail in [9].

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3.3 FPGA APPLICATION MEMORY MAP

Fig.5. shows the memory map for the FPGA area. The FPGA Application Memory Map has an address offset of 64 Mbyte (04000000h).

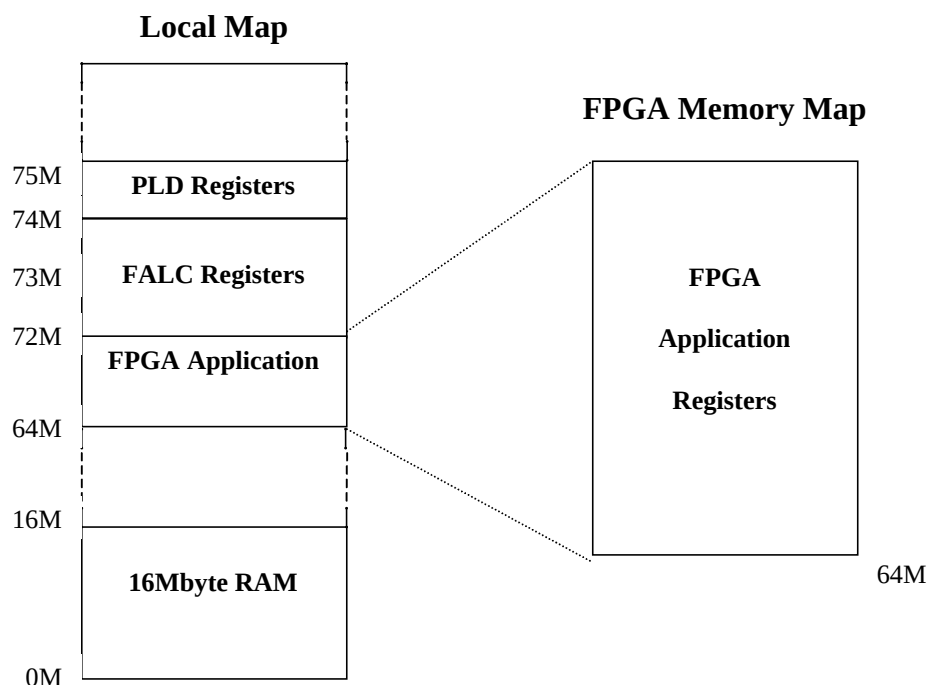


Fig.5. FPGA application memory map

It shall be possible to execute the following functions:

- Reset FPGA Application
- Reconfigure FPGA
- Reset QuadFALC

To use these functions, control registers must be implemented in the FPGA application.

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4 RESET

It is possible to implement four different kinds of reset:

- Reset QuadFALC
- Reset FPGA application from host application
- Reset FPGA to a ready to load application state
- Total reset of the PCB.

The first three resets mentioned above can be set by writing to specific registers in the FPGA Application memory map, see 3.3. A total reset is performed if reset is initiated from the PCI bus via the PCI 9054.

4.1 RESET QUADFALC

The reset pin on the FALC chip is connected to the FPGA, through the PLD, where it can be independently reset from the host application or from the FPGA application. The host application writes to a register in the FPGA Application Memory Map, see 3.3. The FPGA Application then simply activates the reset pin on the FPGA as shown in Fig.6.

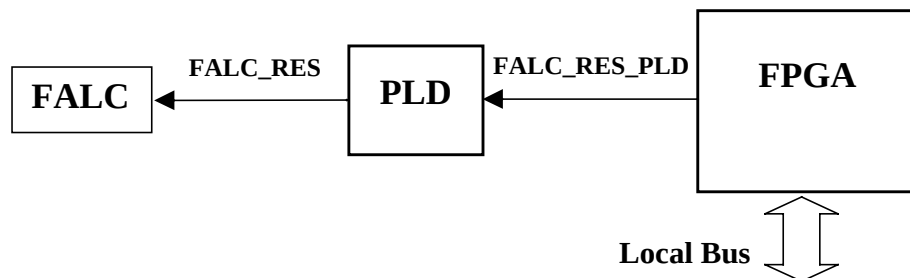


Fig.6. QuadFALC reset

The QuadFalc can also be reset from the PCI9054 via the local bus by signal LRESETo# regardless if the FPGA is configured or noted, see 4.4.

4.2 RESET FPGA APPLICATION FROM HOST APPLICATION

The host application can reset the FPGA application by writing to a reset application register in the FPGA Application Memory Map described in 3.3. When this register is set, the FPGA Application resets itself internally. How the reset is implemented only concerns the FPGA Application and is therefore not discussed any further here.

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4.3 RESET FPGA TO A READY TO LOAD APPLICATION STATE

The host application can reset the FPGA to a ready to load application state by writing to the reconfigure FPGA register in the FPGA Application Memory Map described in 3.3. The FPGA application is responsible for activating the RECONF signal to the PLD. The reconfiguration procedure is described in 7.3.

4.4 TOTAL RESET OF THE PCB

A total reset (see Fig.7.) of the PCB includes:

- Reset PCI 9054. (Set bit 30 of the PCI9054 register located at PCI address offset 6Ch).
 - Reset FPGA to a ready to load application state
 - Reset QuadFALC
1. The PCI interface is reset from the host.
 2. This activates the reset signal LRESETo# on the PCI 9054.
 3. The PLD starts the reset procedure for the QuadFALC.
 4. The PLD also starts the reconfiguration procedure for the FPGA.

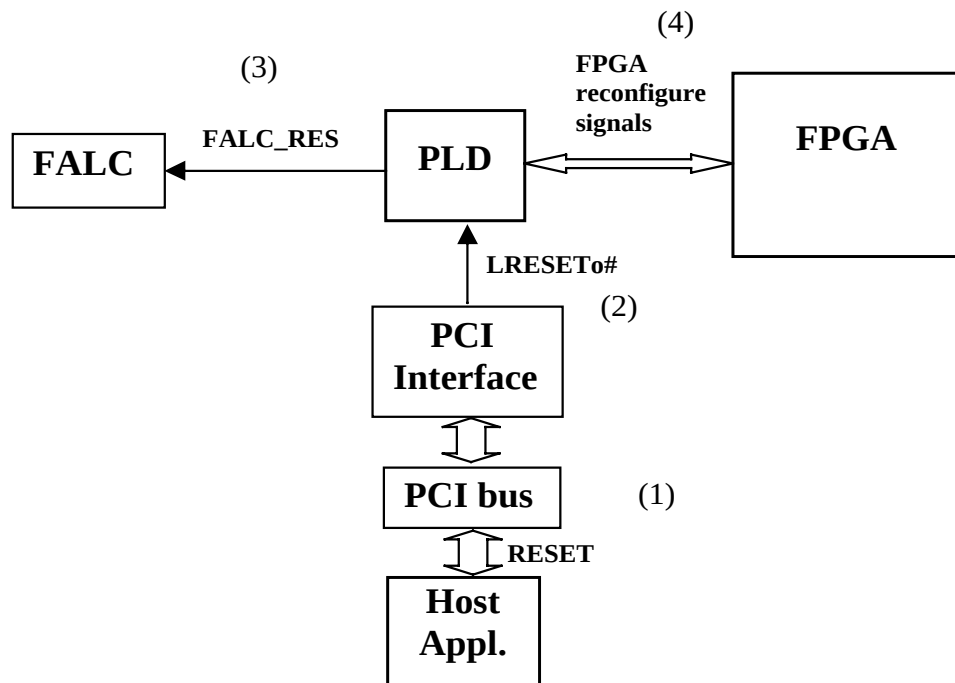


Fig.7. Total reset of the board

The PLD software implementation is described in [3].

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INTERRUPT

All interrupt signals are connected to the FPGA, i.e.

- FALC_INT from QuadFALC
- LINT# to/from the PCI 9054

The interrupt signals are internally routed to the FPGA application.

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TIME BASE

The time base distributes clock signals to a number of components on the PCB. It must be able to phase lock on a clock signal from the QuadFALC (not shown in Fig.8.), extracted from the data on the incoming PCM lines, or from the SCbus.

If there is no data present on the MUX inputs, the VCXO should be able to free run at a frequency of 65.536MHz +/- 32ppm. The time base will therefore consist of five different units: MUX, Phase Detector, Filter, VCXO and Prescaler as shown in Fig.8. The MUX is implemented by EIN in the FPGA. The Phase Detector and the Prescaler is implemented in the PLD and is described in detail in [3].

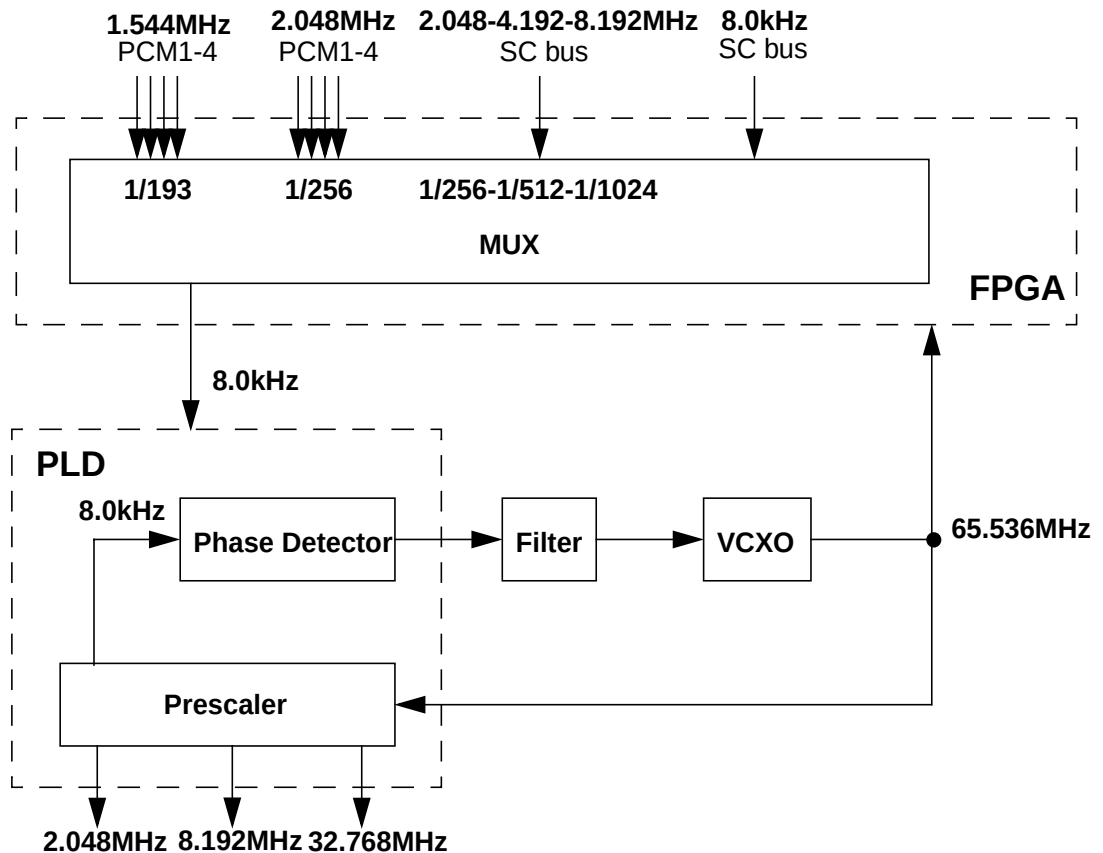


Fig.8. Time Base

The FPGA Application controls which clock source to use. The MUX makes sure that the correct clock source is chosen and divided to an 8.0kHz signal. A control signal to the VCXO is generated by the Phase Detector via an analogue filter to make sure that the 65.536MHz clock signal from the VCXO and the source clock is phase-locked. The phase locked 65.536MHz clock

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signal is then routed to the dedicated clock pins on FPGA and the PLD. In the PLD, the clock is divided to four lower frequencies, those are:

- 8.000kHz for the PLL to lock on.
- 2.048MHz to the QuadFALC.
- 8.192MHz for the FPGA configuration clock.
- 32.768MHz to the PCI9054 and the FPGA.

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7 FPGA CONFIGURATION

Configuration is the process of downloading code into the FPGA. The FPGA has a number of different configuration modes (detailed information can be found in [13]), but the ones used in this application are Slave Serial mode and Boundary-scan mode.

7.1 CONFIGURATION MODE

The Slave Serial mode is used when the FPGA should be loaded from the host via the PCI interface. Data is then written to PLD which loads the FPGA. Data is written to the PLD byte-wise into the FPGA Configuration register (see 3.1) and from there shifted serially into the FPGA.

This is the normal procedure but it is also possible to choose boundary-scan mode. A special download program from Xilinx is then utilized. A download cable is connected from the PC to the P12 connector where the JTAG signals are connected. Three dedicated pins on the FPGA are used to select configuration mode, M2, M1 and M0, see Table 1.

M2	M1	M0	Configuration mode
1	1	1	Slave Serial

Table 1. Configuration modes.

The three mode pins have internal pull-up resistors, and default to logic High if left unconnected. Thus Slave Serial mode is enabled if the mode pins are floating, see Fig.9. Boundary-scan mode overrides the other modes.

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7.2

CONFIGURATION SIGNALS

The signals that need to be routed from the FPGA to the PLD in order to make a Slave Serial configuration are summarized in Table 2. All signals are dedicated except RECONF.

FPGA pin	Signal Name	Direction	Function
RECONF	Reconfigure FPGA	Out	When indicated by the host, the FPGA initializes a reload by pulling RECONF high. The PLD then starts the proper procedure for reconfiguring the FPGA.
CCLK	Configuration Clock	Bidir.	Configuration clock. Input in slave mode.
PROG#	Program	In	Initiates a configuration sequence when asserted low.
DONE	Done	Bidir.	Indicates the completion of the configuration process. Also indicates that the start-up sequence is in progress.
M2, M1, M0	Mode	In	Configuration mode selection.
DIN	Data In	In	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input.
INIT#	Initialisation	Bidir.	When low, indicates that the configuration memory is being cleared. Becomes an I/O after configuration

Table 2. FPGA Slave Serial mode configuration signals.

All configuration signals except M2, M1 and M0 will be connected to the PLD for possible future implementations.

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The signals that need to be routed from the FPGA to the JTAG connector (via the PLD and the QuadFALC to form a chain) in order to make a Boundary-scan configuration are shown in Table 3. All signals are dedicated.

FPGA pin	Signal Name	Direction	Function
TMS	Test Mode Select	In	Boundary-scan controller
TCK	Test Clock	In	Boundary-scan clock
TDI	Test Data Input	In	Boundary-scan data input
TDO	Test Data Output	Out	Boundary-scan data output

Table 3. Boundary-scan mode configuration signals.

7.3 CONFIGURATION DURING RUNNING

Reconfiguration during running can be initialized in one of three ways:

- 1 The host application writes in the Reconfigure FPGA register, described in 3.3, which makes the RECONF signal go active (This register is implemented by EIN).
- 2 The FPGA Application activates the RECONF signal.
- 3 After a total reset of the PCB as described in 4.4.

7.4 CONFIGURATION PROCEDURE

The configuration signals will go active in the following order (From the PLD's point of view):

- 1 The PLD pulls PROGRAM# low in order to clear the FGPA. The FPGA activates INIT#.
- 2 The PLD releases PROGRAM# after >200ns. The FPGA will now clear itself one more time and then release INIT# after 0.1 - 10ms.
- 3 The FPGA samples the mode signals M2-M0 which are high (Slave mode).
- 4 Load data from PCI 9054 and shift it serially into the FPGA. Continue until FPGA is full. (DONE goes high).
- 5 End of slave configuration.

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FPGA COMPATIBILITY

Since the FPGA can be configured with any kind of application in future implementations, there must be a possibility to use a higher density FPGA if needed. This board will use XCV600 utilizing the BG432 package. If higher density is necessary, the XCV800 can be used. These FPGAs need 2.5V power supply internally and 3.3V for the I/Os.

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9 BUS SIGNALS

9.1 LOCAL BUS

The signals needed in the local bus (see Fig.1.) are summarized in Table 4.

Symbol	Signal Name	Function
LA(31:2)	Address Bus	Address Bus
LD(31:0)	Data Bus	Data Bus
LHOLD	Hold Request	Asserted to request use of local bus. The local bus arbiter in the FPGA asserts LHOLDA when control is granted.
LHOLDA	Hold acknowledge	Asserted by local bus arbiter in the FPGA when control is granted in response to LHOLD.
ADS#	Address Strobe	Indicates a valid address and start of a new bus access. Asserted for first clock of a bus access.
LW/R#	Write/Read	Asserted low for reads and high for writes.
BLAST#	Burst Last	Signal driven by current local bus master to indicate last transfer in a bus access.
LBE#(3:0)	Byte Enables	The four byte enables indicate which of the four bytes are active during a data cycle: BE3# Byte Enable 3-LD[31:24] BE2# Byte Enable 2-LD[23:16] BE1# Byte Enable 1-LD[15:8] BE0# Byte Enable 0-LD[7:0]

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Symbol	Signal Name	Function
READY#	Ready	When the PCI9054 is bus master, indicates read data on the bus or write data transfer is complete. When a local bus access is made to PCI9054, indicates read data on bus is valid or a write data transfer is complete.
CCS#	Chip Select	Chip Select to PCI 9054 configuration registers.
LCLK	Local Clock	Local clock input of 32.768MHz.

Table 4. Local bus signals

The following signals to/from the PCI9054 will also be connected to the FPGA for possible future implementations:

Inputs: BIGEND#, BREQi, DREQ[1:0]#, USERI.

Outputs: BREQO, DMPAF/EOT#, LLOCKO#, LSERR#, USERO.

Input/Output: LEDon/LEDin, USERi(I)/DACK0#(O)/LLOCKi#(I), USERo(O)/DREQ0#(I)/LLOCKo#(O).

Bidirectional: BTERM, DP[3:0], WAIT#.

All signals are described in detail in [10].

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9.2 QUADFALC BUS

The signals needed in the QuadFALC bus (see Fig.1.) are summarized in Table 5.

Symbol	Signal Name	Function	From
LA(11:2)	Address Bus	Address Bus	Local Bus
LD(7:0)	Data Bus	Data Bus	Local Bus
FALC_CS#	Chip Select	Chip Select	FPGA
FALC_RD#	Read Enable	Asserted low for reads	FPGA
FALC_WR#	Write Enable	Asserted low for writes	FPGA

Table 5. QuadFALC signals

All signals are described in detail in [9].

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9.3 SDRAM MEMORY BUS

The signals needed in the memory bus (see Fig.1.) are summarized in Table 6. All signals in the bus are connected between the FPGA and the two SDRAM.

Symbol	Signal Name	Function
MA(13:0)	Address Bus	Address Bus and Bank Select
MD(31:0)	Data Bus	Data Bus
SDRAMA_CS#	Chip Select	Chip Select for SDRAM A
SDRAMB_CS#	Chip Select	Chip Select for SDRAM B
SDRAM_RAS#	Row Address Strobe	Indicates row address
SDRAM_CAS#	Column Address Strobe	Indicates column address
SDRAM_WE#	Write Enable	Asserted low for write, high for read
SDRAMA_DQMU	Output disable / Write Mask	Upper byte enable for SDRAM A
SDRAMA_DQML	Output disable / Write Mask	Lower byte enable for SDRAM A
SDRAMB_DQMU	Output disable / Write Mask	Upper byte enable for SDRAM B
SDRAMB_DQML	Output disable / Write Mask	Lower byte enable for SDRAM B
SDRAM_CLK	Clock Input	Clock input of 65.536MHz
SDRAM_CKE	Clock Enable	Clock Enable

Table 6. SDRAM signals.

All signals are described in detail in [14].

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10 CIRCUIT CONNECTOR INTERFACES

10.1 PCM INTERFACE

10.1.1 Pin Configuration

The PCM interface consists of four USB type A connectors, one for each channel. The pin configuration for the four connectors are the same and is shown in Table 7.

Position	Function
1	Receive-
2	Receive+
3	Transmit-
4	Transmit+

Table 7. PCM interface pin configuration

Adaptation cables are delivered with the board and for cable specifications, see [11, 12].

10.1.2 Electrical Characteristics

For electrical characteristics, see [9].

10.2 PCI INTERFACE

For pin configuration and electrical and mechanical specifications, see [10].

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10.3 JTAG INTERFACE

The JTAG signals can be found in PMC connectors P1 and P2 or in test points TP1-TP4. The JTAG signals are shown in Table 8. The PLD, the QuadFALC and the FPGA will be connected to the interface and thus form a JTAG chain.

Test point	Position in connector	Function
TP1	5 (P2)	TDI
TP4	4 (P2)	TDO
TP2	3 (P2)	TMS
TP3	1 (P1)	TCK

Table 8. JTAG interface pin configuration

10.4 CASCADING INTERFACE

The cascading interface, SCbus, can connect up to 32 physical PCBs.

The maximum load on any one SCbus signal shall not exceed 15pF (including connector) per board.

The physical length of the bus shall not exceed 533mm (21 inches).

The connector, named P4, is described in [17].

Further details about the SCbus can be found in [15].

10.4.1 Cascading Interface Signals

All signals on the cascading interface will be connected to the FPGA. That is:

SD_0-SD_15, FSYNC#, SCLK, SCLKx2#, SL_1, SL_3, User I/O1-16, MC, CLKFAIL, SREF8K, SL_4#, SL_2#, SL_0#, CLK8K_IN (user I/O 17), CLK8K_OUT (user I/O 18), ENUM# (user I/O 19), User I/O20-32.

10.4.2 Data Line Termination

SD_0-SD_15, FSYNC#, SCLK, SCLKx2#, SREF8K, CLK8K_IN and SCLK8K_OUT shall all be pulled up to +3.3V by a 33kOhm resistor.

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CLKFAIL shall be pulled up to +3.3V by a 4.7kOhm resistor.

10.5 PMC INTERFACE

The board will use the P1, P2 and P4 connectors as described in [11].

P1 and P2 contains the PCI bus and P4 contains the SCbus.

11 EEPROM

The PCI 9054 must be configured after power-up and after reset for proper behaviour. This is done from an EEPROM. The contents of the EEPROM is shown in [8] and more information about the PCI 9054 registers can be found in [10].

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POWER SUPPLY

The board will rely on power supply from the host via the PMC connector specified in [17]. Most components on the board will require +3.3V but the FPGA needs a core voltage of +2.5V. Two switched voltage regulators residing on the board will convert +5V to +3.3V and +3.3V to +2.5V, see Fig.9.

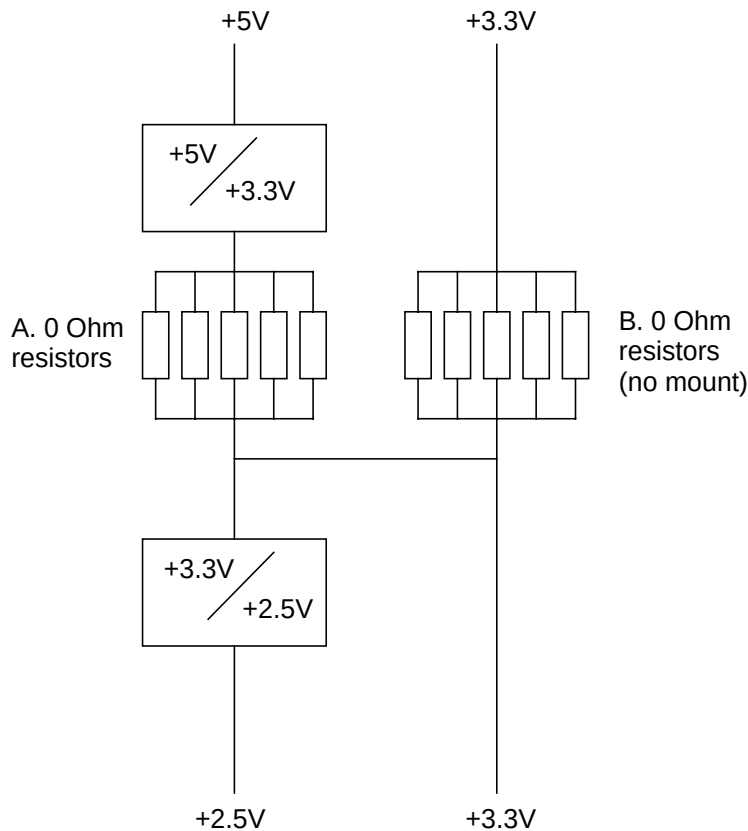


Fig.9. The power supply.

On older mother boards which the SS7-PMC board might be attached to, it is possible that only +5V will exist. Therefore, by default, the A-resistors will be mounted. Current mother boards will most likely have both +5V and +3.3V power supply. On future mother boards, it possible that only +3.3V power supply will exist. In that case, the B-resistors will be mounted instead.

The reason for having five resistors connected in parallell is because the resistors might have as high resistance as 0.05 Ohms. In case of the +5V/+3.3V-converter, it is designed to deliver a maximum of 3.6A load current. With only one resistor, the voltage drop could be as big as $3.6 \cdot 0.05 = 0.18\text{V}$. With five resistors in parallel it will only be $0.18/5 = 36\text{mV}$.

In case of the +3.3V/2.5V-converter, it is designed to deliver a maximum of 2.5A load current.

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MECHANICS

The board will have the physical format shown in Fig.10. PMCs are 149.0x74.0mm. The component envelope maximum height is 8.2mm and the I/O envelope is 13.5mm. The maximum depth of the I/O envelope is 31.0mm. For details, see [17]

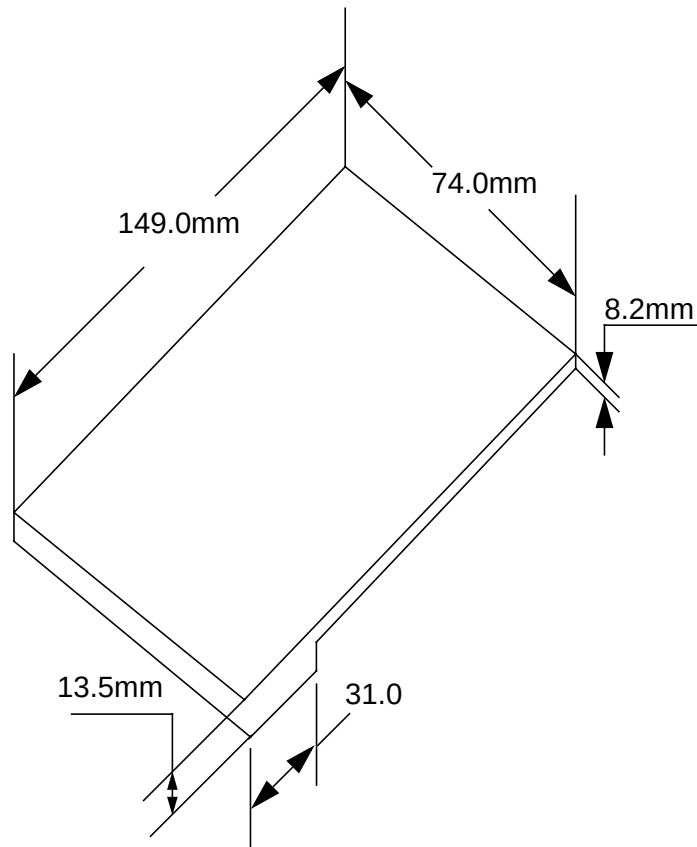


Fig.10. The PCB format.

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TERMINOLOGY

#	Indicates Active Low Signal
BAR	Base Address Register
BGA	Ball Grid Array
BNC	Bayonet Nut Connector
CMC	Common Mezzanine Card
CPLD	Complex Programmable Logic Design
E1	2.048 Mbit/s compliant to ITU G.703
EEPROM	Electrically Erasable Programmable Read Only Memory
EIN	Ericsson Infotech, Karlstad
EMC	Electromagnetic Compliance
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group. IEEE 1149.1 boundary scan.
LSB	Least Significant Bit
MUX	Multiplexer
N.C.	No Connect
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCM	Pulse Code Modulation
PLCC	Plastic Leadless Chip Carrier
PLD	Programmable Logic Design
PLL	Phase-Locked Loop

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		File	

PMC	Pci Mezzanine Card
QuadFALC	Quad Frammer And Line Interface Component
RJ	Registered Jack
SDRAM	Synchronous Dynamic Random Access Memory
SS7	Signalling System 7
T1	1.548 Mbit/s compliant to ITU G.703
VCXO	Voltage Controlled Crystal Oscillator
VHDL	Very High Speed Integrated Circuit Hardware Description Language

Table 9. Terminology