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Approved UAB/Y/DT Tomas Jonsson	Checked	Date 2001-03-15	Rev A	Reference NSP HW

PENTIUM III CPCI-MXP64 PROCESSOR AND MOTHER/ADAPTER BOARD COMBINATION FOR GEM

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GENERAL

The purpose of this design specification is to define the base conditions required for the physical design of the combination cPCI-MXP64 Pentium III (ROF 366 810/1) processor board and a mother/adaptor board combination that adapt to the form factor and the interfaces of the General Ericsson Magazine, GEM.

The mother/adaptor boards provide the following functions:

- Termination of the duplicated -48V
- Conversion from -48V to +12V, +5V and +3.3V
- Duplicated Ethernet 100Base-TX access
- I2C M-bus interface for board identity and MIA-led
- Board and subrack address
- Power down
- Insertion sense

The Pentium III processor hard disk option is not utilized.

The plug-in unit including the Pentium III processor is 30 mm wide.

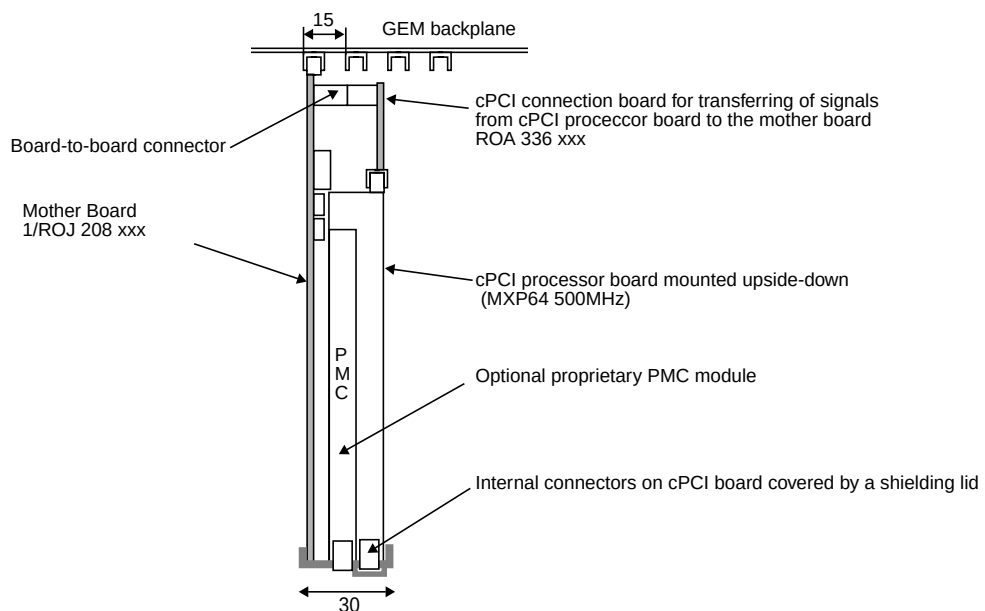


Fig.1. Adapter/mother boards for a single slot cPCI processor

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1.1 OTHER PENTIUM PROCESSORS

The mother/adaptor board is custom-made for the MXP64 Pentium III processor and no other cPCI board can be used.

1.2 HISTORY

Rev PA1 is the first revision.

Rev PA2 12V (+/-) regulator added, chapter 2.2. Board interconnection pins added, chapter 3.9

Rev PA3 Revision remarks from 2000-01-26 corrected (2.2.1, Fig.9, 3.7.4, 3.8.1, 3.8.2, 5.1, 5.2.)

Rev PA4 Table 10 and Table 11 updated. Table 14 new. Table 15-21 renumbered and new Table 15 also changed.

Rev A Updated nomenclature. Fig.2, paragraph 2.4.1 and Table 8 updated according to increased address possibility.

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2 FUNCTIONAL DESCRIPTION

2.1 BLOCK DIAGRAM

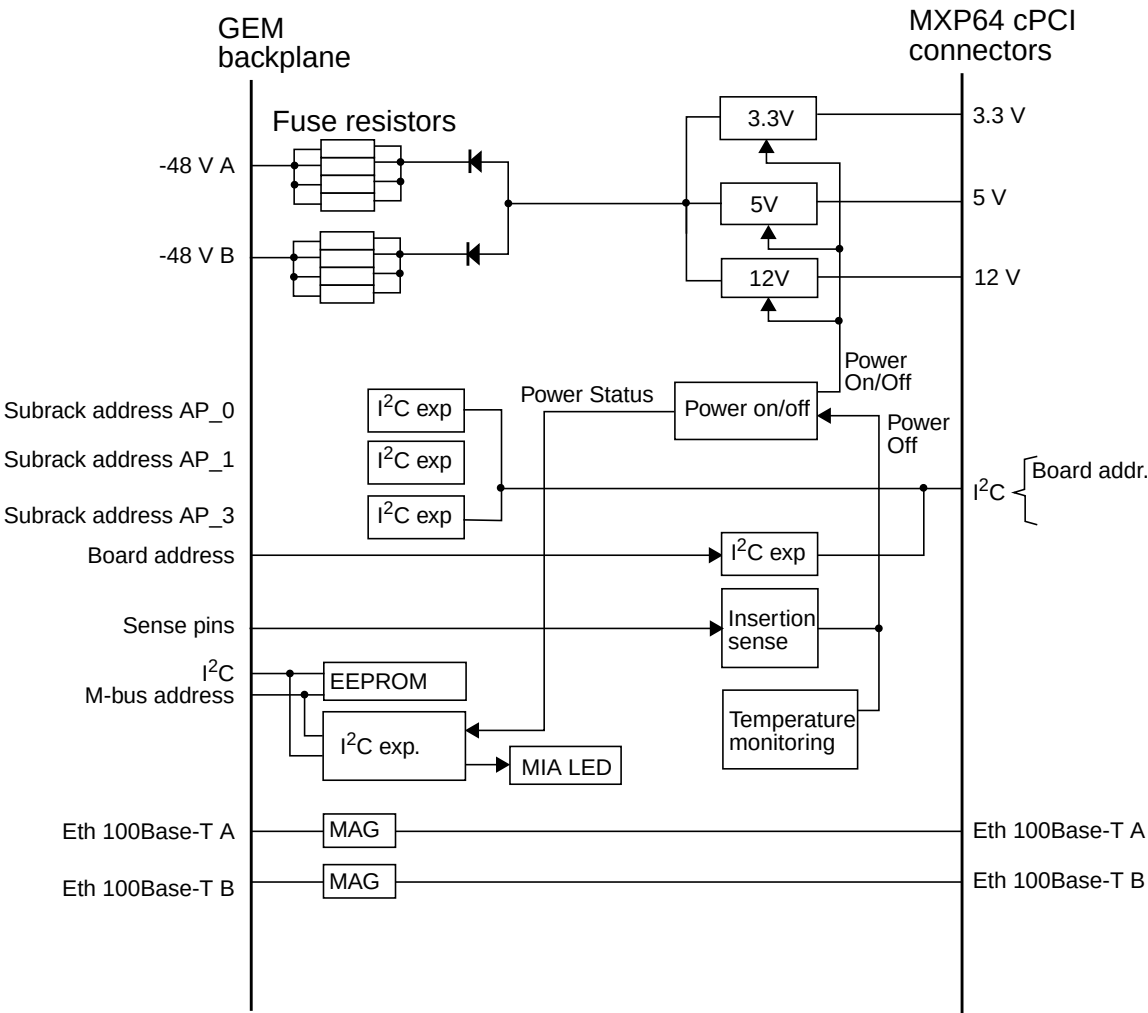


Fig.2. Pentium MXP64 mother/adapter block diagram

2.2 POWER SUPPLY

Power are supplied from the GEM backplane to the mother/adapter boards through a 1 ohm fuse resistor and a diode in series from each -48VDC branch. (See Fig.2.)
Four REP670 in parallel are used for the 1 ohm fuse resistor.

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Table 1. MXP64 Pentium III estimated power consumption

Low Power, 500 MHz	Power dissipation typical [W]	Power dissipation maximum [W]
768 MByte SDRAM		30
>1 GB		~30

Mother/adaptor boards power consumption: ~ 1W

This is achieved with three DC/DC modules.

Synqor PQ48033QNA25NKS +3.3VDC @ 25A, Efficiency: 87%

Synqor PQ48050QNA20NKS +5VDC @ 20A, Efficiency: 89%

RYT 913 6001/C +/- 12VDC @ 0.5A, 6W out, Efficiency: >80%

2.2.1 +5V/+3.3V DC/DC Heat Dissipation

The MXP64 Pentium III 500 MHz processor board with memory needs three voltages:

3.3V @ maximum 5.0A

5V @ maximum 3.2A

12V @ maximum 20 mA

Power dissipation is below the levels calculated for CP1500 in RNS which means no heat sink is calculated. Maximum contribution from PMC is estimated to 7W. No extra power dissipation anticipated due to increased memory to 1 GB.

2.2.2 CPU thermal management

The purpose of this function is to protect the MXP64 board from destruction at high temperature without losing more functionality than necessary by throttling the CPU speed.

The CPU temperature of the MXP64 board is monitored both on die and case level. The throttling temperature, as well as the resume full speed temperature, can be set individually for die and case supervision. A minimum of 4 degrees hysteresis is always ensured.

2.2.3 Fail Safe Power On/Off

There is also a requirement of an "only hardware" temperature on/off switch. This device is a temperature sensor/switch placed on the mother board and connected to the on/off function of the DC/DC converters. The shutdown

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temperature is chosen as to prevent ambient temperature within board combination to reach beyond 74 °C. The DC/DC converters shall automatically restart when the ambient temperature is lowered.

As signals are lost when power is lost it means that the power on/off function must be fed from the -48V directly from the backplane and an edge triggered or a latched set/reset device will be used that is independent and insensitive of the power down/up sequence on the signal line or other disturbances on the power feeding.

The status of the power on/off device shall be possible to read out from the maintenance bus.

The board shall always start at hot insertion or when the subrack power is switched on.

The insertion sense mechanism function is also connected to this device. For more information see insertion sense chapter.

2.3 MEMORY

Maximum configuration limit for MXP64 on board main memory shall be at least 1 GB. (Note! Not possible with present model of MXP64.)

2.4 ADDRESS INFORMATION

The processor board shall be able to read subrack and board/slot address.

2.4.1 Subrack Address

The subrack address is defined by address plugs AP_0, AP_1 and AP_3 mounted in dedicated subrack positions. Each plug can have 16 different address configurations, represented by four bits plus parity. The subrack address is available at each slot in the GEM backplane. For protection, each GEM plug-in unit shall have Schottky diodes (RKZ 323 102/1).

At present, the GEM subrack address is given by AP_0 (4 bits). Due to the need of a larger address space, the GEM address will be defined be AP_1 plus AP_3 (8 bits).

In order to cope with both addressing methods, the MXP64 shall be able to read the subrack address pins from all three address plugs. Fig.3 shows the subrack address implementation for MXP64. The address lines are connected to I2C expanders on the adapter and read into the MXP64 via the I2C bus on the cPCI connector J1.

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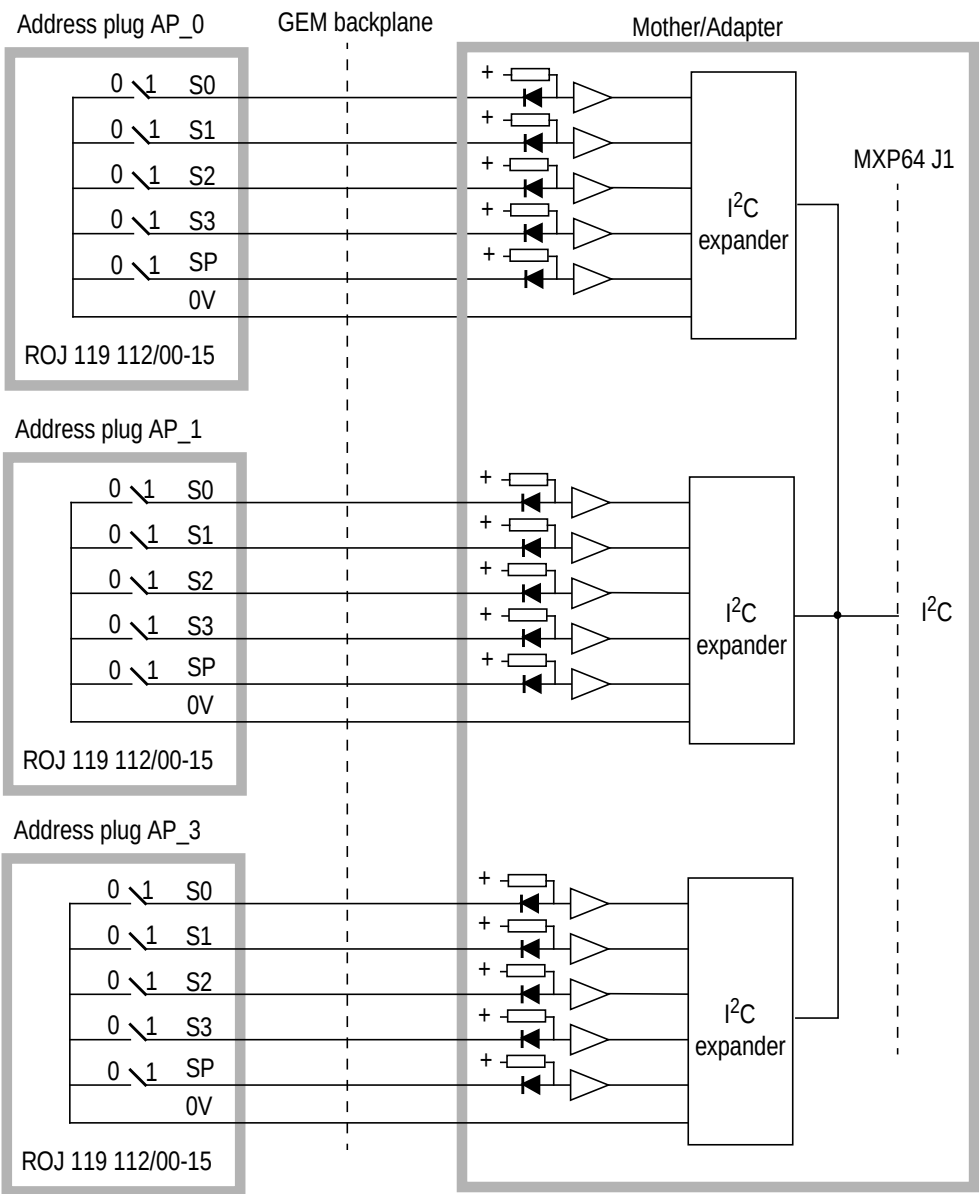


Fig.3. Subrack address implementation

2.4.2 Board/Slot address

Board addresses are numbered from 0 to (n-1) for each available slot from left to right in the GEM.

The board address is taken from the backplane for each board. An address pin connected to ground in the backplane = "0". An open circuit address pin = "1". Five address pins and one parity pin are used, which allows 32 boards to be addressed see Fig.4. Odd parity is used.

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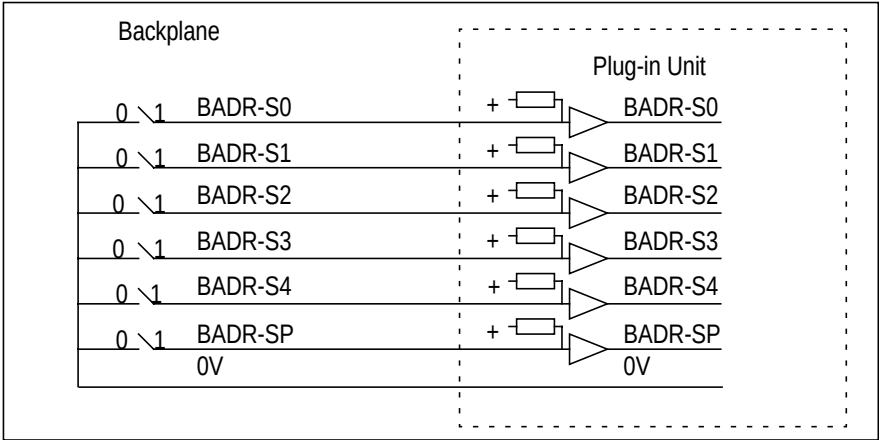


Fig.4. Board address implementation

The address lines are connected to an I2C expander on the mother/adapter boards and taken into the MXP64 via the I2C bus on the cPCI connector J1.

2.5 PMC OPTION

It shall be possible to include one PMC (ROA 209 21/1) at MXP64.

2.6 INSERTION SENSE

For each device board there are two backplane connectors, one in the top and one in the bottom, that have shorter pins. There is a connection in the backplane between the pins. The MXP64 board will not be powered up before these pins are properly connected. This means that the -48V must be used for the logic circuit as the power modules are off.

The status of the insertion sense device controls the power modules. The joint status of the power modules is possible to read out from the maintenance bus.

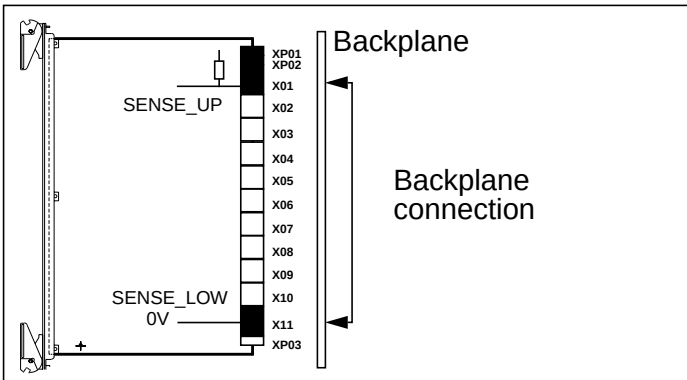


Fig.5. Insertion sense implementation

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2.7 MAINTENANCE BUS

The maintenance bus is implemented as a I2C bus. The SCB-RP acts as a master of this bus. The bus is single and not implemented with redundancy. The maintenance function on each device board in GEM is powered and supervised by the SCB-RP board.

The device board address is hard-coded in the backplane. An address pin connected to ground in the backplane is equal to “0” and an open pin is equal to “1”. A0 is the least significant bit.

Board/slot address and maintenance bus address do not use the same physical backplane pins due to separated power supplies.

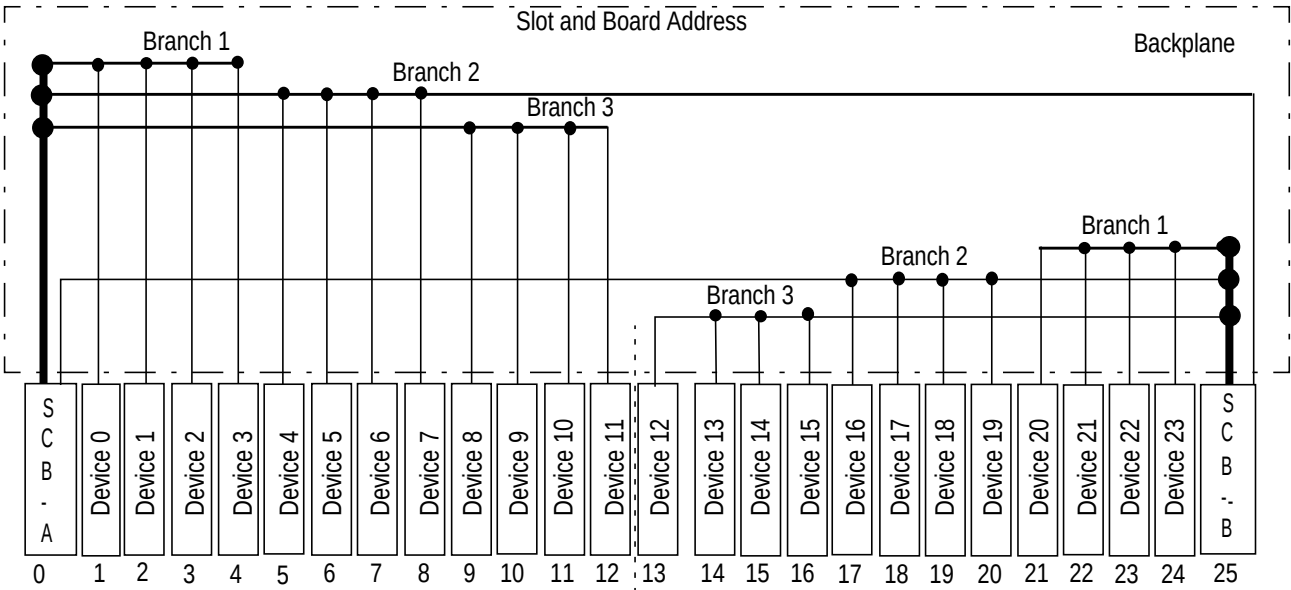


Fig.6. M-bus implementation

Table 2. M-bus address

Slot in GEM M-bus address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Physical position	02	08	11	14	17	20	23	26	29	32	35	38	41	44	47	50	53	56	59	62	65	68	71	74	77	80
MB_A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
MB_A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
MB_A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
MB_A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1

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Slot in GEM M-bus address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Physical position	02	08	11	14	17	20	23	26	29	32	35	38	41	44	47	50	53	56	59	62	65	68	71	74	77	80
MB_A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
SCB - A branch >	-	1	1	1	1	2	2	2	2	3	3	3	3	-	-	-	-	-	-	-	-	-	-	-	-	2
SCB - B branch >	2	-	-	-	-	-	-	-	-	-	-	-	-	3	3	3	3	2	2	2	2	1	1	1	1	-

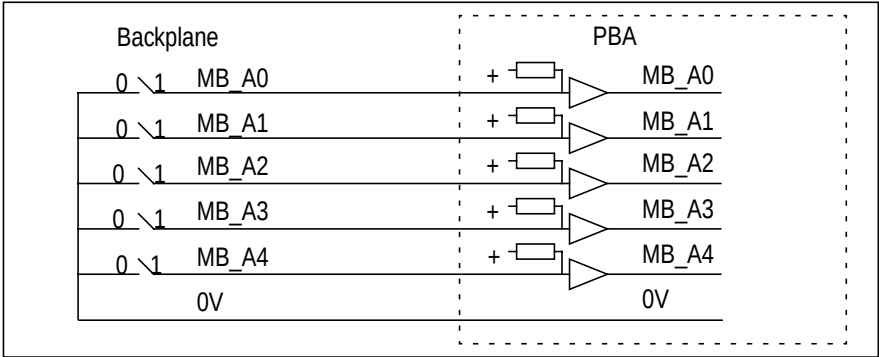


Fig.7. Maintenance bus address implementation

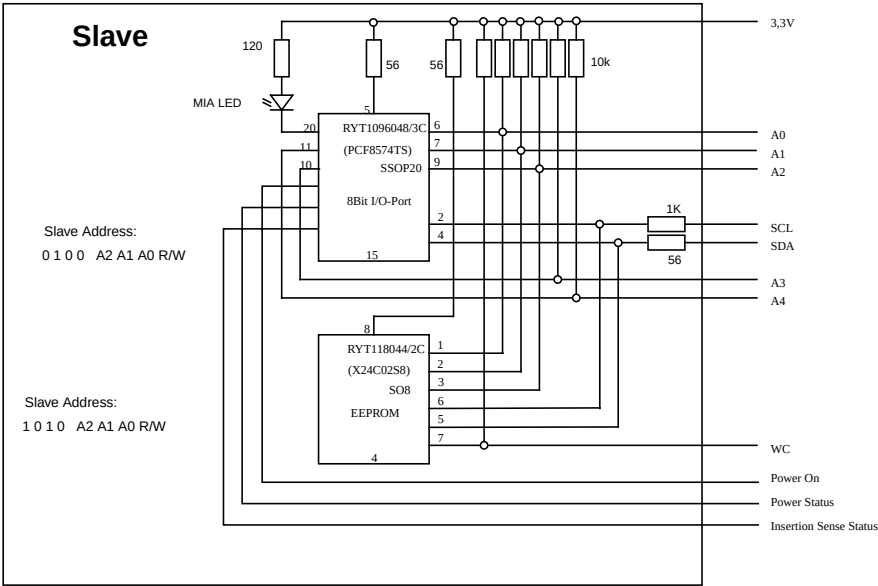


Fig.8. Device board maintenance bus interface

As the MIA-led is mounted on the mother board there is a plastic light guide to convey light to the front panel.

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2.8 SERIAL INTERFACE

Serial RS232/V24 connection with a 9 pin D-Sub at the front shall be possible.

2.9 ETHERNET INTERFACE

The MXP64 shall support two Media Independent Interfaces (MII) accessible via the cPCI J2 connector.

3 MECHANICAL DESIGN

3.1 FRONT PANEL DESIGN

No front panel needed for MXP64. Serial RS232 connection shall be possible through mother front when trouble shooting. This hole in the front has to be covered to fulfil EMC requirements.

3.1.1 Front Panel Dimensions

T.B.D

3.2 ADAPTER BOARD DIMENSIONS

Adapter board is built on PCB TVK 336.

3.3 MOTHER BOARD DIMENSIONS

Mother board shall fit a standard GEM 30 mm wide PCB slot (TVJ 828).

3.4 PCB CHARACTERISTICS

Table 3: PCB Characteristics

Board		Comments
Thickness [mm]	1.66+/-0.2 mm	
Number of Layers	8	
Number of Signal -Layers	4	
Technology		
Impedance	single ended: 70 Ohm balanced: 100 Ohm	

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Table 3: PCB Characteristics

Board		Comments
Width [mil]	5	
Conductor [pattern class]	54	
Conductor spacing [pattern class]	54	
Land pattern class	55	
Remarks	None	
Risks	None	

3.5 ADAPTER AND MOTHER INTERCONNECTION

The connection between mother and adapter will be located in the same way as for the ROJ 208 401/1, CP1500 in RNS, in an attempt to keep these two solutions as similar as possible.

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3.6 CPCI AND GEM CONNECTOR DESIGNATION/ALLOCATION

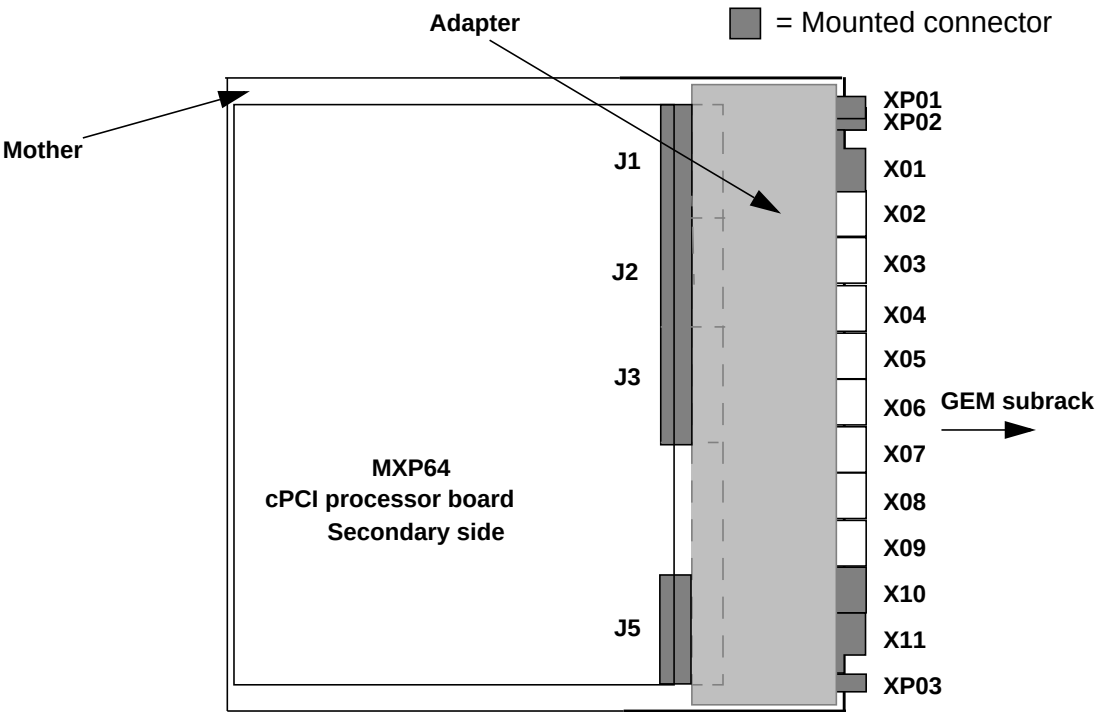


Fig.9. Mother/Adapter cPCI and GEM connector configurations

3.7 GEM CONNECTOR PIN ALLOCATION

3.7.1 Power Supply

All power are supplied trough a two blade power contact (4pins/blade) one for each branch. The connectors are placed in the top of the magazine. Pin number 1-4 are always GND.

Table 4. DEV XP01 and XP02

Acronym	Full name	Connector	Pin
GND	GND branch A1(2)	XP01	1,2,3,4
-48V_A	-48V, branch A1(2)	XP01	5,6,7,8
GND	GND, branch B1(2)	XP02	1,2,3,4
-48V_B	-48V, branch B1(2)	XP02	5,6,7,8

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3.7.2 Maintenance Bus

Table 5. Device slot pin-out X01

Acronym	Full name	Connector	Pin
MB()_SCL<n>	Serial Clock	X01	A04
MB()_SDA<n>	Serial Data	X01	B03
MB()_3V	3.3 V	X01	B04
MB_WC	Write control	X01	B01
MB_A0	Address A0	X01	A02
MB_A1	Address A1	X01	B02
MB_A2	Address A2	X01	D02
MB_A3	Address A3	X01	E02
MB_A4	Address A4	X01	A03

() = A or B

3.7.3 Insertion Sense

Table 6. Insertion sense X01 and X11 pin-out

Acronym	Full name	Connector	Pin
SENSE_U	SENSE Upper	X01	A01
SENSE_L	SENSE Lower	X11	A10

3.7.4 Ethernet

Table 7. Ethernet pin out 100Base-T on X10

Acronym		Full name	Connector	Pin_P	Pin_N
100BaseTA_TXP_()	100BaseTA_TXN_()	Transmit Data A	X10	A01	B01
100BaseTA_RXP_()	100BaseTA_RXN_()	Receive Data A	X10	A02	B02
100BaseTB_TXP_()	100BaseTB_TXN_()	Transmit Data B	X10	E01	D01
100BaseTB_RXP_()	100BaseTB_RXN_()	Receive Data B	X10	E02	D02

() = 0 - 25

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3.7.5 Subrack Address

Table 8. Subrack Address on X10 and X11.

Acronym	Full name	Connector	Pin
AP_0-S0	AP_0 address, bit 0	X10	A06
AP_0-S1	AP_0 address, bit 1	X10	B06
AP_0-S2	AP_0 address, bit 2	X10	D06
AP_0-S3	AP_0 -address, bit 3	X10	E06
AP_0-SP	AP_0 even parity	X10	E05
AP_1-S0	AP_1 address, bit 0	X11	A01
AP_1-S1	AP_1 address, bit 1	X11	B01
AP_1-S2	AP_1 address, bit 2	X11	D01
AP_1-S3	AP_1 address, bit 3	X11	E01
AP_1-SP	AP_1 even parity	X11	A02
AP_3-S0	AP_3 address, bit 0	X11	B02
AP_3-S1	AP_3 address, bit 1	X11	D02
AP_3-S2	AP_3 address, bit 2	X11	E02
AP_3-S3	AP_3 address, bit 3	X11	A03
AP_3-SP	AP_3 even parity	X11	B03

3.7.6 Board/Slot Address

Table 9. Board address pin-out on X11

Acronym	Full name	Connector	Pin
BADR-S0	Board address, bit 0	X11	D03
BADR-S1	Board address, bit 1	X11	E03
BADR-S2	Board address, bit 2	X11	A04
BADR-S3	Board address, bit 3	X11	B04
BADR-S4	Board address, bit 4	X11	D04
BADR-SP	Board address, odd parity	X11	E04

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3.7.7 JTAG

Table 10. JTAG connector 01

Acronym	Full name	Connector	Pin
GEM_BS_TCK	Test Clock	X01	D01
GEM_BS_TMS	Test Mode Select	X01	E03
GEM_BS_TDI	Test Data Input	X01	D03
GEM_BS_TDO	Test Data Output	X01	D04
GEM_BS_TRSTZ	Test Reset	X01	E01
ASP_BYPZ		X01	E04

3.8 MXP64 CPCI PIN ALLOCATION

3.8.1 MXP64 J1 connector

Table 11. MXP64 J1 Connector

TeknorAcronym	Full name	Connector	Pin
VCC3E	3.3V	J1	A15,17,19,21,23 C06,10,18,22 D25
VI/O	5V/3.3V selectable	J1	C04,08,16,20,24
VCCE	5V	J1	A01,25 B02,24 D03,23 E01,25
-12VE	-12V	J1	B01
+12VE	+12V	J1	D01
GND	Ground	J1	B06,08,10,16,18,20,22 D05,07,09,11,17,19
IPMB_SCL	Management Bus-Clock	J1	B17
IPMB_SDA	Management Bus-Data	J1	C17
RST#	Reset	J1	C05

All other pins in J1 are no connect.

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3.8.2 MXP64 J2 connector

Table 12. MXP64 J2 Connector

Teknor Acronym	Full name	Connector	Pin
V/I/O	5V/3.3V selectable	J2	A04 C05,07,09,11,13
GND	Ground	J2	B01,03,07,09,11,13,15,17 D04,06,08,10,12,14,16,18,20

All other pins in J2 are no connected.

3.8.3 MXP64 J3 connector

Table 13. MXP64 J3 Connector

Teknor Acronym	Full name	Connector	Pin
VCC	5V	J3	B03,08,13 C08 D12
+12V	+12V	J3	D10 E10
GND	Ground	J3	A02,08,10 B05,11 C02 D05 E01,02,09
ETX-0		J3	A03
ETX+0		J3	A05
ERX-0		J3	C04
ERX+0		J3	C05
ETX-1		J3	B09
ETX+1		J3	A09
ERX-1		J3	D09
ERX+1		J3	C09

All other pins in J2 are no connected.

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3.8.4 MXP64 J5 connector

Table 14. MXP64 J2 Connector

Teknor Acronym	Full name	Connector	Pin
VCC	5V	J5	B13

3.9 BOARD INTERCONNECTION PIN ALLOCATION

Table 15. X101 Connector

Pin	Row A	Row B	Row C	Row D
01				TSRT 1)
02			TMS 1)	
03	PLD_TDO 1)		I2C2_SCL	
04			I2C2_SDA	
05			TCK 1)	
06	TDO 1)			

1) Not fully implemented. Not supported by MXP64.

Table 16. X102 Connector

Pin	Row A	Row B	Row C	Row D
01	ETX-0	ETX+0	ERX-0	ERX+0
02				
03				
04				
05				
06	ETX-1	ETX+1	ERX-1	ERX+1

Table 17. X110 Connector

Pin	Row A	Row B	Row C	Row D
01	+5V	3.3V	nc	0V
02	+5V	3.3V	nc	0V
03	+5V	3.3V	nc	0V
04	+5V	3.3V	nc	0V
05	+5V	3.3V	nc	0V
06	+5V	3.3V	nc	0V

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Table 18. X111 Connector

Pin	Row A	Row B	Row C	Row D
01	+5V	3.3V	nc	0V
02	+5V	3.3V	nc	0V
03	+5V	3.3V	nc	0V
04	+5V	3.3V	nc	0V
05	+5V	3.3V	nc	0V
06	+5V	3.3V	nc	0V

Table 19. X112 Connector

Pin	Row A	Row B	Row C	Row D
01	+5V	3.3V	nc	0V
02	+5V	3.3V	nc	0V
03	+5V	3.3V	nc	0V
04	+5V	3.3V	nc	0V
05	+5V	3.3V	nc	0V
06	+5V	3.3V	nc	0V

Table 20. X113 Connector

Pin	Row A	Row B	Row C	Row D
01	+5V	3.3V	nc	0V
02	+5V	3.3V	nc	0V
03	+5V	3.3V	nc	0V
04	+5V	3.3V	nc	0V
05	+5V	3.3V	nc	0V
06	+5V	3.3V	nc	0V

Table 21. X114

Pin	Row A	Row B	Row C	Row D
01	+12V	nc	-12V	0V
02	+12V	nc	-12V	0V
03	+12V	nc	-12V	0V
04	+12V	nc	-12V	0V
05	+12V	nc	-12V	0V
06	+12V	nc	-12V	0V

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4 VERIFICATION AND TEST

To support Boundary Scan through the mother/adaptor board a JTAG access that complies with IEEE 1149.1 can be implemented. The purpose would be to test MXP64 and mother/adaptor together. No more Boundry Scan circuit would be included.

If the MXP64 board shall be included in the test chain is an open question.

JTAG is available on the X11 connector of The GEM backplane.

5 ENVIRONMENTAL REQUIREMENTS

5.1 DEPENDABILITY

Technical lifetime: > 20 years

MTBF > 10 years (MXP64 + mother/adaptor boards)

5.2 TEMPERATURE

According to reference /2/, the MXP64 + mother/adaptor boards shall fulfil the following temperature ranges (ambient temperature at PBA position):

Normal operation: +5 °C to +55 °C

Safe operation: -5 °C to +65 °C

Non destruction: -10 °C to +70 °C

5.3 EMC

The MXP64+mother/adaptor boards shall comply with the requirements stated in reference /1/.

5.4 ESD

The MXP64+mother/adaptor boards shall comply with the requirements stated in reference /1/.

Prepared (also subject responsible if other)		No. 102 62-ROJ 208 405/1 Uen		
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6 REFERENCES

6.1 SOURCE DOCUMENTS

- /1/ EMC Generic Requirements; EN/LZB 118 16Uen, Rev.R4;
- /2/ General Requirements for AXE10 telecommunication equipment practice; 1/1056-FCP 105 280Uen, Rev. C; 96-03-28.
- /3/ P-BIST Design for Testability Rules; 1520-FDB 111 02Uen, Rev. B; 97-11-27; ETX/U/VK Claz Angelbro.
- /4/ Requirement Specification for the Pentium Processor in the GEM APZ 302 System; 1056-ROJ 208 103/1, Rev. A.