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Test Instructions for GESB ROJ 208 410/1

Document History

Describe the document changes below.

Date	From	To	Changes and reason for changes
01-07-26		A	First Release
02-12-20	A	B	Updated for GTM

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1 Introduction

This document is a test instruction for the system test of the, ROJ 208 410/1, GESB board (Ref. [1]).

2 Test object

Test is valid for: ROJ 208 410/1
ROJ 208 410/2

3 Test Sequence

The test is divided into three parts: Initial test, System test and Switch test. All three parts are shortly described below.

3.1 Initial Test

This is a test of RAM and it is executed before the GESB starts up. If test passes the GESB boots in a normal way and execution of test programs can start. If test fails Ethernet is initiated from DPRAM and test result can be fetched from board to GTM.

3.2 System Test

System test itself is divided into tree parts: Maintenance Bus Test, DEST and Gigabit Ethernet Test. The tests are shortly described below.

3.2.1 Test of Maintenance bus

This is a test of maintenance bus in GEM (Ref. [2]). The SCB-RP provides the maintenance bus interface. This is implemented as a normal I²C bus. The SCB-RP acts as the master on this bus, but has also a slave interface like all other boards in the GEM magazine. The maintenance bus also gives the possibility to point out specific PBA in a magazine by controlling the MIA-LED. The test of maintenance bus is to turn the MIA-LED on and off on GESB board in GEM. Also programming of the IDPROM is a test of maintenance bus. The test runs from test GTM (General Test Manager).

3.2.2 DEST

DEST (Downloadable Ethernet based Self-Test) is used for memory tests, FIA processor interface test and read/write operation to certain components connected to processor or FIA. DEST on GESB also set up the Gigabit Ethernet Switch for communication. DEST is divided into 12 subtests. Subtest 1-5 is general for all PBA's using the RPI-block and 7 subtest are specific for the GESB. Each of them performs test of some functionality on the PBA or does some necessary set ups used by other subtest. All subtests are briefly described in table 1.

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Table 1: Subtest in DEST for GESB

Subtest	Name of the subtest	Description
	Test of RPI-block	
1	FIA	Test of FIA ASIC, Ctrl logic, addr & data bus
2	Short RAM test	Test of RAM
3	Long RAM test	Test of RAM
4	Temp sensor	Test of temperature sensor in RPI-Block
5	ReadPos	Read out board position and subrack ID
	Test of GESB	
6	Setup	Settings for QSPAN in MPC860
7	QSPAN	Test of interface between QSPAN and MPC860
8	Init PCI	Initiation of PCI interface, BCM5680 - QSPAN
9	BCM5680	Test of interface between BCM5680 and QSPAN
10	Init BCM5404	Initiation of PHY:s
11	BCM5404	Test of PHY:s
12	Interrupt	Test of interrupt between BCM5680, QSPAN and MPC860

The DEST downloads and executes from the GTM. If an error appears the DEST generates an error message that reports what part of the test failed, and some more error information

3.2.3 Test of Gigabit Ethernet Switch

This part test, the Gigabit Ethernet Switch on GESB board. GESB provides eight 1000Base-T ports towards the front. The test is to run some DEST test on the GESB when the Ethernet traffic is looped via the front connectors on the GESB board.

3.3 Switch Test

To verify that the board boots up and start running after programming of OS and PBOOT a switch test is performed. The test is to send Ethernet traffic trough all ports in the front of GESB. This is a similar test like the Gigabit Ethernet Test.

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4 Requirements

4.1 Required material

Qty	Article	Name
1	BFD 508 002/1	GEM
2	ROJ 208 323/2	SCB-RP
1	ROJ 208 410/1	GESB (Test objects)
1	-	Test PC
1	-	TFTP-server
1	-	Switch
2	-	Network Cable for switch test
2	TSR 491 0274	Ethernet straight (for switch)
4	TSR 490 0101/1	-48V

I.e. a GTM Platform

For cables see reference [4].

4.2 Software

Article	Name
CXC 105 189	GTM (<i>Test GUI</i>) Reference [3]
CXC 105 188	EBOOT on all PBA's in GEM.
CXC 105 217	DEST for GESB

I.e. Software for GTM

OS and PBOOT for GESB: See 1095-ROJ 208 410 for actual version of board.

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5 Set ups before test

5.1 Hardware preparation before test

Place two SCB-RP boards in GEM (in slot 0 and 25). Place the number of GESB boards in the magazine in free positions. It is possible to test up to 12 GESB boards at the same time.

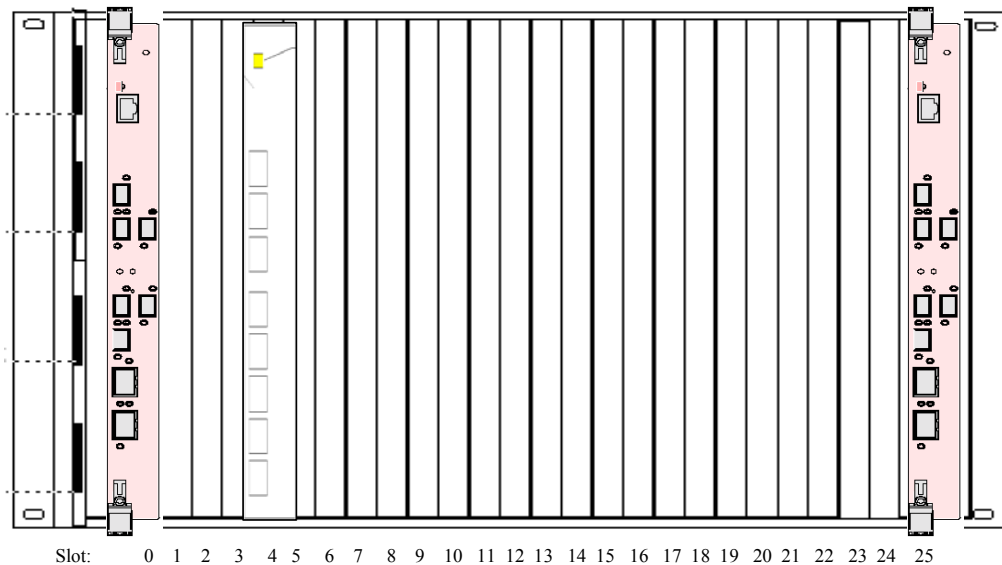


Figure 1. GEM with two SCB-RP boards and one GESB board.

Connect the SCB-RP boards to power. Connect the SCB-RP board from the Switch to one of the Ethernet ports in the front of the SCB-RP board. (connection from the switch see figure 2).

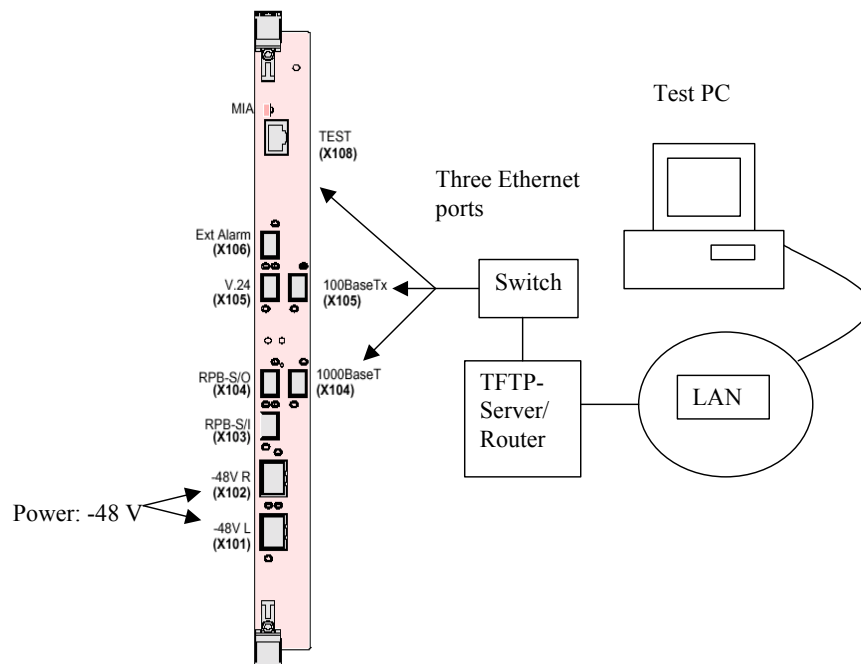


Figure 2. External connections of power and test equipment for SCB-RP.

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5.2 Setting IP-addresses

Ethernet address for a PBA in GEM depends on three things, magazine, slot and left or right SCB-RP. The Ethernet address looks like 192.168.X.YZZ. The first numbers are hard coded in EBOOT, X is the number of the upper address plug in the GEM, Y is 1 if the left SCB should be used and 2 if it is the right SCB and ZZ is the slot number plus 1.

Example: The left SCB-RP in a GEM (slot 0) with number 4 on the upper address plug has the IP-addresses 192.168.4.101 and 192.168.4.201.

6 Test sequence

6.1 Initial Test

After power up, the processor makes a complete RAM test on the board.

This RAM test will take some time.

If test passes the board boots in a normal way and execution of system test can start.

If test fails Ethernet is initiated from DPRAM.

Test result is then fetched from the board by GTM. See reference [5] for information on fault codes during power up.

6.2 System Test

System test is divided in tree parts.

6.2.1 Test of Maintenance bus

This is a test of the maintenance bus in GEM. The test is executed from GTM.

The test of the maintenance bus is done by turning the MIA-LED on and off on GESB and to program and verify the ID-prom.

6.2.2 DEST

This is a self-test on the GESB. The test downloads to GESB from GTM. GTM is described in reference [4]. The DEST is placed on the TFTP-server from with the GTM can fetch the program.

The test program number, run by GTM, can be any of the test numbers specified in table 1 page 3. That is test 1-5 for RPI part and test 6-12 specific for SCB.

These tests are also combined into test sequences, numbered 101-104, and runs automatic in GTM. Test flow 101 runs subtest 1-6 (test of RPI and set up of QSPAN). This test flow runs during start up of test. Test flow 102 runs 7-12 (Set up of Switch). This test flow runs once to initiate the switch. After this subtest all ports in the front works in Gigabit Ethernet mode. Test flow 103 is test of the switch and run subtests 6,10-12. This test flow runs during Gigabit Ethernet Test. Test flow 104 runs subtest 1-5, 7, 11, 12. This test flow is for heat test. After test check the messages for correct slot and address plug is OK. If there are one or more errors, the test failed. See below what different error codes mean. Otherwise if there is no error, the test has passed.

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6.2.2.1 Subtest details

Subtest 1-6 is for all boards with RPI-core. Subtest 1-9 is for the mother board and subtest 10-17 is for the daughter board.

Subtest 1

Test of interface between CPU and FIA ASIC.

Index 1

Data bus stuck fault and opens test. Write and read 0's and 1's at lowest and highest address.

If there is a fault, the following error code is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 2: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 2

Walking '1' for FIA SRAM (data).

If there is a fault, the following error codes is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 3

Walking '0' for FIA SRAM (data).

If there is a fault, the following error codes is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 4

Address bus stuck faults, opens and shorts test. Walking '1' and '0' for FIA SRAM.

If there is a fault, the following error codes is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 2: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 3: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 4: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 5: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 6: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 5

March test of SRAM. Enable the internal FIA SRAM, and define the start address at 0xD0000000.

No test is performed in this subtest.

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Index 6

March test of SRAM. Read background 0x00 and write 0xFF.

If there is a fault, the following error code is issued:

Error code 1: March test on FIA internal SRAM failed at address 0xXX.

Index 7

March test of SRAM. Read background 0xFF and write 0x00.

If there is a fault, the following error code is issued:

Error code 1: March test on FIA internal SRAM failed at address 0xXX.

Index 8

March test of SRAM. Read background 0x00.

If there is a fault, the following error code is issued:

Error code 1: March test on FIA internal SRAM failed at address 0xXX.

Index 9

Checkerboard test of SRAM. Write background 0xAA at even addresses and 0x55 at odd addresses.

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on FIA internal SRAM failed at address 0xXX.

Index 10

Checkerboard test of SRAM. Write background 0x55 at even addresses and 0xAA at odd addresses.

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on FIA internal SRAM failed at address 0xXX.

Index 11

March test of RPBSIC in FIA. Write background 0x00.

No test is performed in this subtest.

Index 12

March test of RPBSIC in FIA. Read background 0x00 and write 0xFF.

If there is a fault, the following error code is issued:

Error code 1: March test on RPBSIC in FIA failed at address 0xXX.

Index 13

March test of RPBSIC in FIA. Read background 0xFF and write 0x00.

If there is a fault, the following error code is issued:

Error code 1: March test on RPBSIC in FIA failed at address 0xXX.

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Index 14

March test of RPBSIC in FIA. Read background 0x00:

If there is a fault, the following error code is issued:

Error code 1: March test on RPBSIC in FIA failed at address 0xXX.

Index 15

Checkerboard test of RPBSIC in FIA. Write background 0xAA at even addresses and 0x55 at odd addresses

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on RPBSIC in FIA failed at address 0xXX.

Index 16

Checkerboard test of RPBSIC in FIA. Write background 0x55 at even addresses and 0xAA at odd addresses

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on RPBSIC in FIA failed at address 0xXX.

Subtest 2

Short memory test.

Tests the data bus and the address bus.

It is divided into 5 indexes, all of them described below.

Index 1

Data bus stuck fault and opens test. Writing 0's to the lowest address and 1's to the highest, and then reading the values back do this.

If there is a fault, the following error codes is issued:

Error code 1: Cannot write to lowest address in DRAM.

Error code 2: Cannot write to highest address in DRAM.

The values read back is printed out along with what was expected.

Index 2

This test checks if the data bus (32 bits) to DRAM is OK.

The test is performed using walking 0 and walking 1 tests, this means that one bit on the data bus is set to 0 or 1 and all the other bits is set to the opposite value.

The walking 1 data is sent to the lowest address in DRAM and the walking 0 data is sent to the highest address in DRAM. The data is then read back to verify that the bit value has not changed. The bit is then shifted one step and then the write, read and verify is done all over again, this continue until all bits have been tested.

If there is a fault, the following error codes is issued:

Error code 1: Error when rotating 1 on data-bus. Faulty bits 0XXXXXXXXX

Error code 2: Error when rotating 0 on data-bus. Faulty bits 0XXXXXXXXX

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Faulty data bus bits are reported in “Error detail”, in hex format 0XXXXXXXX, where the X’s represents faulty bits during the test.

E.g. 0x00000003 indicates that the two lowest data bits is faulty.

The information in “Error detail” is also printed in the text message.

Index 3

Address bus stuck fault and opens test. Writing 0xFF to the lowest byte and 0x00 to the highest, and then reading the values back do this.

If there is a fault, the following error codes is issued:

Error code 1: Error when writing to ram base. (Address 0x00000000)

Error code 2: Error when writing to ram top. (Address 0xFFFFFFFF)

The values read back is printed out along with what was expected.

Index 4

DRAM address bus test using walking 1. (32 bits)

This means that the first bit on the address bus is set to ‘1’ and all the other bits is set to ‘0’. Then the test data (0x00) is written to that address and read back to verify that the data has not changed. The data is also compared with the content in ram base. The bit is then shifted one step and then the write, read and verify is done all over again, this continue until all bits have been tested.

If there is a fault, the following error codes is issued:

Error code 1: Error in ram base when rotating 1 on address bus.

Error code 2: Error when rotating 1 at current address.

Error code 3: Error, bits stuck to '0' when rotating 1 on address bus.

Faulty data is reported in ‘Error detail’ and in ‘address’, ‘expected’ and ‘received’. For error code 1 Error detail show the current address tested. ‘Address’, ‘expected’ and ‘received’ show the content of ram base.

For error code 2 Error detail is not used. ‘Address’, ‘expected’ and ‘received’ show the content of the address tested.

For error code 3 faulty address bus bits are reported in “Error detail”, in hex format 0XXXXXXXX, where the X’s represents faulty bits during the test.

E.g. 0x00000003 indicates that the two lowest address bits is faulty.

The information in “Error detail” is also printed in the text message. ‘Address’, ‘expected’ and ‘received’ is not used.

Index 5

DRAM address bus test using walking 0. (32 bits)

This means that the first bit on the address bus is set to ‘0’ and all the other bits is set to ‘1’. Then the test data (0xFF) is written to that address and read back to verify that the data has not changed. The data is also compared with the content in ram top. The bit is then shifted one step and then the write, read and verify is done all over again, this continue until all bits have been tested.

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If there is a fault, the following error codes is issued:

Error code 1: Error in ram top when rotating 0 on address bus.

Error code 2: Error when rotating 0 at current address.

Error code 3: Error, bits stuck to '1' when rotating 0 on address bus.

Faulty data is reported in 'Error detail' and in 'address', 'expected' and 'received'.
For error code 1 Error detail show the current address tested. 'Address', 'expected' and 'received' show the content of ram base.

For error code 2 Error detail is not used. 'Address', 'expected' and 'received' show the content of the address tested.

For error code 3 faulty address bus bits are reported in "Error detail", in hex format 0XXXXXXXXX, where the X's represents faulty bits during the test.

E.g. 0xC0000000 indicates that the two highest data bits is faulty.

The information in "Error detail" is also printed in the text message. 'Address', 'expected' and 'received' is not used.

Subtest 3

Long memory test.

Tests the DRAM circuits.

It is divided into 2 indexes, both of them described below.

For all of the test steps in subtest 3 there is a limit to the number of errors that will be printed out.

Index 1

March test of all address locations. This test is divided into 4 test steps.

1. Write value 0x00000000 at incremented address.
2. Read back value 0x00000000 and write 0xFFFFFFFF at incremented address.
3. Read back value 0xFFFFFFFF and write 0x00000000 at decremented address.
4. Read back value 0x00000000 at incremented address.

If there is a fault, the following error codes is issued:

Error code 1: Error when reading current address. (Test step 2)

Error code 2: Error when reading current address. (Test step 3)

Error code 3: Error when reading current address. (Test step 4)

The address where the fault occurred and the values read back is printed out along with what was expected.

Index 2

Checkerboard test of all address locations. This test is divided into 2 test steps.

1. Write 0xAAAAAAAA to all even addresses and 0x55555555 to all odd addresses, then read back and verify all values.
2. Write 0x55555555 to all even addresses and 0xAAAAAAAA to all odd addresses, then read back and verify all values.

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If there is a fault, the following error codes is issued:

Error code 1: Error when reading current address. (Test step 1)

Error code 2: Error when reading current address. (Test step 2)

The address where the fault occurred and the values read back is printed out along with what was expected.

Subtest 4

Test of temperature sensor LM75 (N5003).

The test is divided into five parts described below.

Index 1

Read out content of the Tos and the Thyst registers and compare them with the default reset values. Default value of the Tos register is 80 degrees Celsius and of the Thyst register is 75 degrees Celsius. The temperature sensor is connected to the CPU via an I2C-interface.

If there is a fault, the following error codes is issued:

Error code 1 Tos register does not contain the programmed value of 80 degrees Celsius in N5003!

Error code 2: Thyst register does not contain the programmed value of 75 degrees Celsius in N5003!

Index 2

Write 100 degrees Celsius to the Tos register and 90 degrees Celsius to the Thyst register.

No test is performed in this index.

Index 3

Read out content of the Tos and the Thyst registeters and compare them with the "should-be-values" which were set in the Index 2, i.e. 100 degrees Celsius for Tos and 90 degrees Celsius for Thyst.

If there is a fault, the following error codes is issued:

Error code 1 Tos register does not contain default value of 100 degrees C in N5003!

Error code 2: Thyst register does not contain default value of 90 degrees C in N5003!

Index 4

Write 80 degrees Celsius to the Tos register and 75 degrees Celsius to the Thyst register. These are the default values (see Index 1) and should be restored.

No test is performed in this index.

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Index 5

Read out content of the Tos and the Thyst registers and compare them with the values written in Index 4.

If there is a fault, the following error codes is issued:

Error code 1 Tos register does not contain the programmed value of 80 degrees Celsius in N5003!

Error code 2: Thyst register does not contain the programmed value of 75 degrees Celsius in N5003!

Subtest 5

Read out board position and subrack ID

Index 1

This test reports four messages to GTM with information of what value the tree address plugs and board position in the GEM magazine. Check that these values are correct.

If there is a fault, the following error codes is issued:

Error code 1: Parity error for AP0 check address plug in upper position in GEM

Error code 2: Parity error for AP1, check address plug in middle position in GEM!

Error code 3: Parity error for AP2, check address plug in lower position in GEM!

Subtest 6

Set up for applications connected to the RPI-core.

Index 1

Settings for QSPAN in MPC860..

Subtest 7

Test of QSPAN. Read and write to some registers in QSPAN.

Index 1

Read from the QSPAN_PCI_ID, expected data 0x086210E3.

If there is a fault, the following error codes is issued:

Error code 1: Read from QSPAN (D4) failed!

Index 2

Write to the QSPAN_PCI_ID.

If there is a fault, the following error codes is issued:

Error code 1: Write to QSPAN (D4) failed!

Error code 2: Write to QSPAN (D4) failed!

Error code 3: Write to QSPAN (D4) failed!

Error code 4: Write to QSPAN (D4) failed!

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Subtest 8

Initiations of PCI interface in QSPAN and BCM5680.

Index 1

Initiations of PCI interface in QSPAN.

No test is performed in this index.

Index 2

Set up of PCI interface in BCM5680

No test is performed in this index.

Subtest 9

Test of BCM5680.

Index 1

Read from the Revision Information Register (RO) in BCM5680, expected data 568014E4.

If there is a fault, the following error codes is issued:

Error code 1: Read from BCM5680 (D100) failed!

Index 2

Read from EPC_PFM0 in BCM5680, expected data 55555555.

If there is a fault, the following error codes is issued:

Error code 1: Read from switch BCM5680 (D100) failed, no acc. back!

Error code 2: Read from switch BCM5680 (D100) failed, wrong data!

Subtest 10

Set up of Switch.

Index 1

Set up of the memory of the Switch.

No test is performed in this index.

Index 2

Set up of registers in the Switch

No test is performed in this index.

Index 3

Set up of registers in the PHY's

No test is performed in this index.

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Subtest 11

Test of the two BCM5404 (D12 and D16).

Index 1

Read from PHY 1-4 (D12)

If there is a fault, the following error codes is issued:

Error code 1: Read from PHY 1 (D12) failed!

Error code 2: Read from PHY 2 (D12) failed!

Error code 3: Read from PHY 3 (D12) failed!

Error code 4: Read from PHY 4 (D12) failed!

Index 2

Read from PHY 5-8 (D12)

If there is a fault, the following error codes is issued:

Error code 1: Read from PHY 5 (D12) failed!

Error code 2: Read from PHY 6 (D12) failed!

Error code 3: Read from PHY 7 (D12) failed!

Error code 4: Read from PHY 8 (D12) failed!

Subtest 12

Test of interrupt in MPC860 from QSPAN and BCM5680

Index 1

Disable all interrupts in mpc860.

If there is a fault, the following error codes is issued:

Error code 1: CPU interrupts not disabled!

Index 2

Check of interrupts in MPC860 from QSPAN and BCM5680.

If there is a fault, the following error codes is issued:

Error code 1: No interrupt generated in MIIM register BCM5680 (D100)!

Error code 2: No interrupts in MPC860!

Error code 3: No interrupt from QSPAN (D4)in MPC860!

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6.2.3 Test of Gigabit Ethernet Switch

The DEST program set up the switch for Gigabit Ethernet traffic. To test that all ports in the front works a test sequence is performed over all ports. The GTM control this test.

The GESB board works on Gigabit traffic. The SCB-RP has one Gigabit Ethernet Port in the front. This port is used to test the switch on GESB. Connect the right SCB-RP board from the switch to the 100tBase port, and then connect the first GESB board in port 1 (input) from the gigabit port on the right SCB-RP board. Connect the gigabit port on the left SCB-RP board in the magazine from port 0 (output) on the GESB board.

It is possible to test more than one GESB at the same time, just make sure that you have all inputs in slot 1 and all outputs in slot 0. Before starting this test in GTM it is a good idea to try to ping the test object from a DOS-prompt to verify the connection before starting the test. After running a test sequence on the first port GTM tells to move all inputs to port 2 on the GESB board. Same test sequence is performed on every port on the GESB.

6.2.4 Requirements after System Test

The GESB board have to be restarted to get rid of the DEST program.

Software like OS, parameters and PBOOT is then to be downloaded to GESB.

These files are placed on the TFTP-server. Then the GESB is restarted again as the last part in System Test. All this is done automatically in GTM.

6.3 Switch Test

This is a test of OS and PBOOT on GESB boards. The test is similar to the Gigabit Ethernet Test (same connections). After loading of PBOOT and OS a test of Ethernet Traffic is performed thru the GESB board. The OS on GESB set up the board for Ethernet traffic but the PBOOT on GESB board don't support Ethernet traffic. So instead of trying to ping the board itself, try to ping the SCB-RP board. This test runs from a DOS-prompt.

7 Faulty boards

If a board don't pass a test, the board serial number, test number, index number, error code and other error data from the fault is written to a log file.

8 Requirements after test

If all tests pass put a label with "SYS OK" on the PBA

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9 Abbreviation

CPU	Central Processor Unit
DEST	Downloadable Ethernet based Self Test
DPRAM	Dual-Port Random Access Memory
EBOOT	Ethernet BOOT
FIA	Support ASIC for the MPC860 processor
GEM	Generic Ericsson Magazine
GESB	Gigabit Ethernet Switch Board
GTM	GEM Test Manager
GUI	Graphic User Interface
I ² C	Inter-Integrated Circuit
PBA	Printed Board Assemble
RP	Regional Processor
SCB	Support and Connection Board
SDRAM	Synchronous Dynamical Random Access Memory

10 References

Ref.	Document name	Document number
1	DS GESB	10262-ROJ 208 410/1
2	DS for GEM	102 62-BFD 508 002/1
3	GTM	1551-CNZ 105 189
4	Cables in GEM	1/0363-3/FCP 105 1003
5	EBOOT	1551-CXC 105 188