Product Description ROJ 208 323/2 SCB-RP

Abstract

This document is the product description of SCB-RP.

Revision information

Revision	Date	Comment
B	02-10-21	Changed from ROJ 208 323/1 to ROJ 208 323/2. The contents is not changed.
A	01-05-16	First version

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1 Purpose

This document covers the implementation of the PIU for the SCB-RP. It is intended to provide sufficient understanding of the SCB-RP so a re-design/modification can be made. Software designers will also find information about registers and memory maps. The description should be read with the schematic diagram reference /10/ and /11/ at hand.

2 Source Documents

/1/ Implementation Proposal of SCB-RP board; 1/159 41 - 4/FCP 105 308Uen, Rev. A; 99-03-19; eedtobi, eedthlu.

/2/ Design Specification of RPIHW1A; 10262-ROZ1011163/1Uen, Rev.PA3;EED/E/X/B Torsten Billwitz.

/3/ Design Description for FIA ; 1551-ROP10112Uen, Rev.B; 2000-04-10; UAB/D/HH Tomas Franden.

/4/ Design Specification of GDM; 102 62-BFD 508 002/1Uen, Rev.PB2;2000-06-27;UAB/X/MM Gunnar Lindström.

/5/ EMC Generic Requirements; EN/LZB 118 16Uen, Rev.R4;

/6/ General Requirements for AXE10 telecommunication equipment practice; 1/1056-FCP 105 280Uen, Rev. C; 96-03-28.

/7/ P-BIST Design for Testability Rules; 1520-FDB 111 02Uen, Rev. B; 97-11-27; ETX/U/VK Claz Angelbro.

/8/ LVDS General Purpose Link; 1.3 IEEE1596.3-1996.

/9/ Product Specification; 1301-TVJ82801Uen, Rev.PA2;2000-10-04; EED/E/P/E T. Billwitz.

/10/ Circuit diagrams of SCB-RP, Mother board, 1911-1/ROJ 208 323 Uen, Rev. A

/11/ Circuit diagrams of SCB-RP, Daughter board, 1911-1/ROJ 208 03 Uen, Rev. A

2.1 Module Specification Documents

/12/ MPC860 User’s Manual, MPC860UM/AD Rev.1.

/13/ Datasheet of BCM5401; 5401-DS04-R; 2000-07-21.

/14/ Datasheet of GT-48303A; Rev.1.0; 2000-04-17.

/15/ Datasheet of GT-48330; Rev.1.0; 99-12-18.

/16/ Datasheet of GT-48350; Rev.1.0; 2000-03-30.

/17/ Datasheet of GT-48360; Rev.1.0; 2000-04-10.

/18/ Datasheet of LXT9784; Rev.1.0; 2000-March.

/19/ RPG Debug Terminal; 1301-SXA 106 3100Uen; Rev. A;98-03-17; UAB/B/RG JOEL

3 General

The SCB-RP board is designed to be used in the GEM. For redundancy reasons each GEM will be equipped with two SCB-RP boards. The SCB-RP plug-in unit is composed of a mother and a daughter board.

The SCB-RP board serves a number of main functions:

- Delivering power (-48V) to all boards in GEM.
- Distributing RPB-S to all boards in GEM.
- SCB-RP is an Ethernet switch, able to handle communication between boards in GEM as well as communication to GEM-external stations.
- SCB-RP houses an RPI.
- SCB-RP is an handler of external alarms.
- SCB-RP is the master on the Maintenance bus

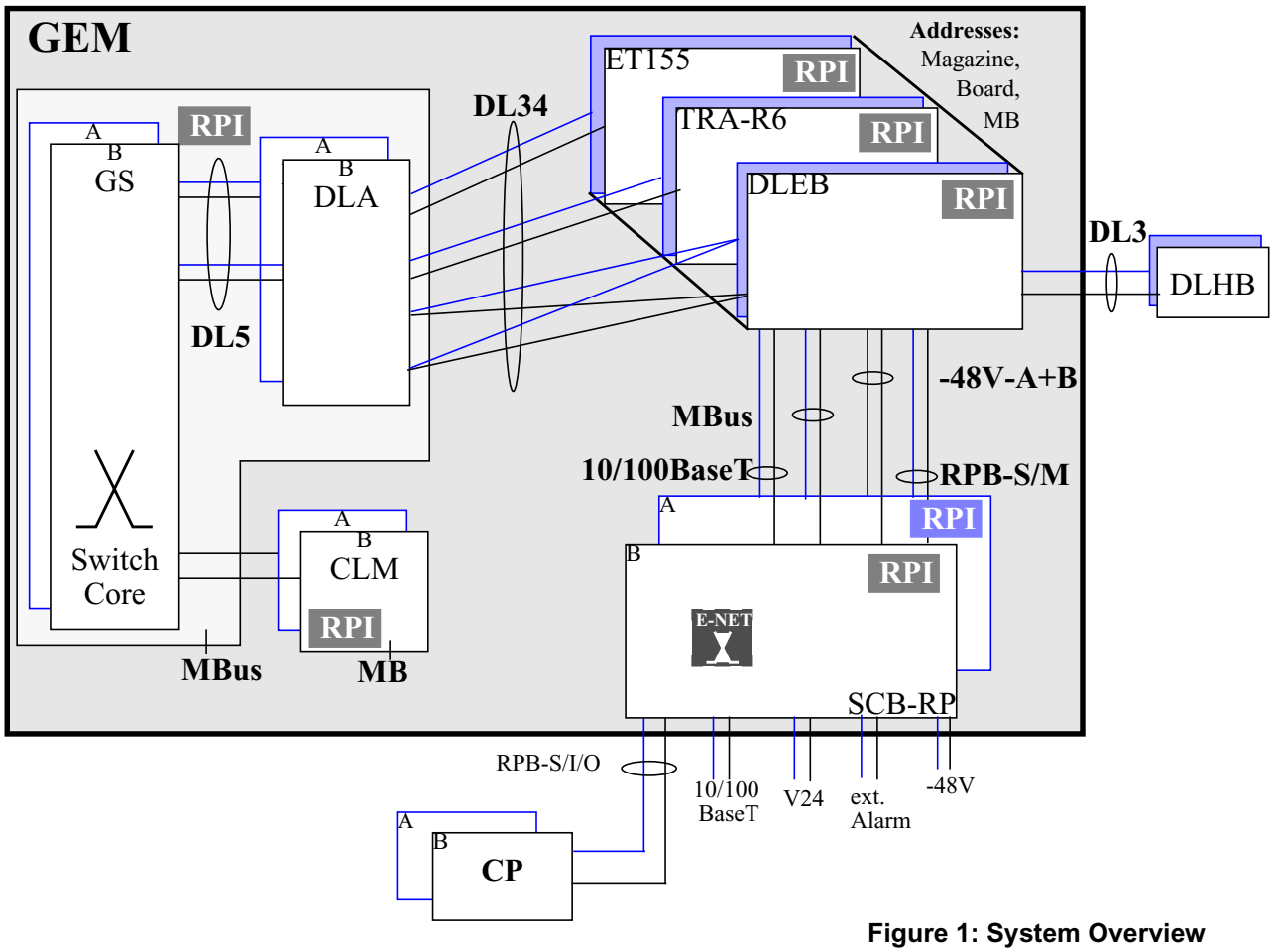


Figure 1: System Overview

3.1 Definitions

1. The words *MPC860P*, *CPU,* and *MPC* are used synonymously and have always the same meaning throughout this document.

4 Functional Description

4.1 Block Description

4.1.1 Block Diagram

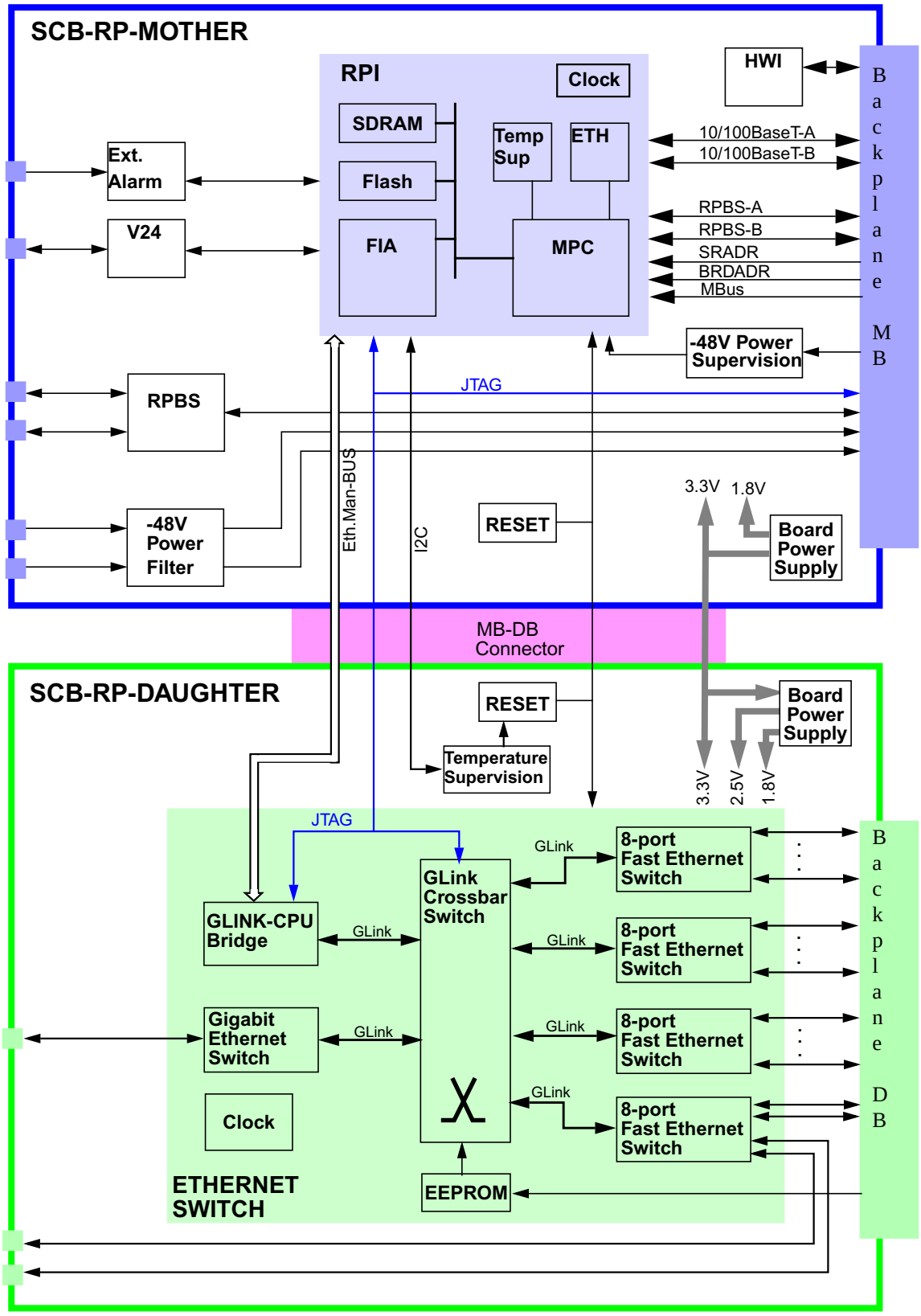


Figure 2: SCB-RP block diagram

4.1.2 RPI

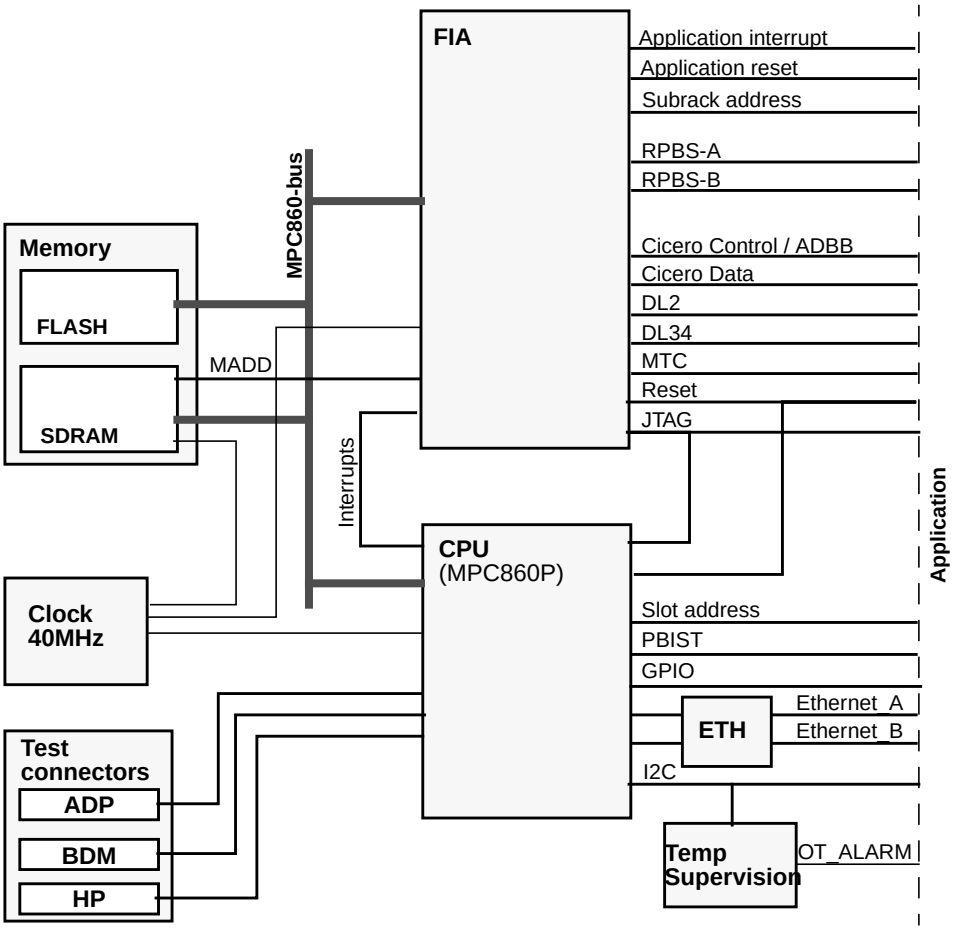


Figure 3: RPIHW1A block diagram

4.1.2.1 CPU

The processor is a MPC860P which is an embedded processor from Motorola. It consists of a 32 bit PowerPC core and a communication processor module, which is controlled by a separate RISC processor. Some of the PowerQUICC's features are:

- 16-Kbyte instruction and 8-Kbyte data cache
- 32-bit data bus (dynamic bus sizing for 8,16, and 32 bits), 32 address lines
- Reset controller
- Interrupt controller
- Memory controller with interface to SRAM, SDRAM and Flash memory
- Memory management unit (MMU)
- Software watchdog
- Several power save modes
- I2C interface

- JTAG / BDM ports

4.1.2.2 FIA

This ASIC will be used as a companion chip to the MPC860 PowerQUICC communication controller.

FIA will have interfaces to the following functions/devices:

- The MPC860 bus with 32-bit address and 32-bit data
- Cicero ASICs
- DL34
- IEEE 1149 JTAG
- MTC IEEE 1149 JTAG (board master test controller)
- The serial RP-bus path A/B in backplane, RPB-S
- ADB (external devices with MPC860 interfaces connected through FIA)
- (DL2 interface is also supported by FIA but it is not part of the RPIHW1A, and for this reason it is not described in this document.)

The MPC860 interface is a both master and slave interface. The FIA is a master when a DMA transaction is taking place controlled by the FIA. FIA will utilize the bus arbiter which is integrated in the PowerQUICC to become a master of the bus.
During SDRAM accesses address multiplexing for row and column addresses is done in FIA The multiplexer is controlled by the signal ‘GPL5’ generated in the MPC860’s memory controller.
FIA also performs parity check and generation, if enabled.

Due to FIA’s limited pin count, ADB and Cicero control bus share pins. Hence, either ADB or Cicero control bus can be used at a time, controlled by a pin ‘ADBB_CICEROZ’.

4.1.2.3 Memory

The memory consist of Random Access Memory (SDRAM) and Flash memory. The memory is connected via the 860-bus to the FIA and to MPC860. In order to maximize the available bandwidth of this bus only fast, low latency devices are used. All slow I/o devices are placed on the MPC860’s communication processor module or on FIA’s ADB.

The MPC860’s memory controller is responsible for controlling the memory devices. The General-Purpose Chip-select Machine (GPCM) provides interfacing to the flashes, while one of the more sophisticated User Programmable Machine (UPM) is used to interface to the SDRAMs. Programming of GPCM and UPM is part of the boot sequence, and is done by PBOOT.
No external glue logic is needed except a multiplexer for row and column addresses of the SDRAMs.

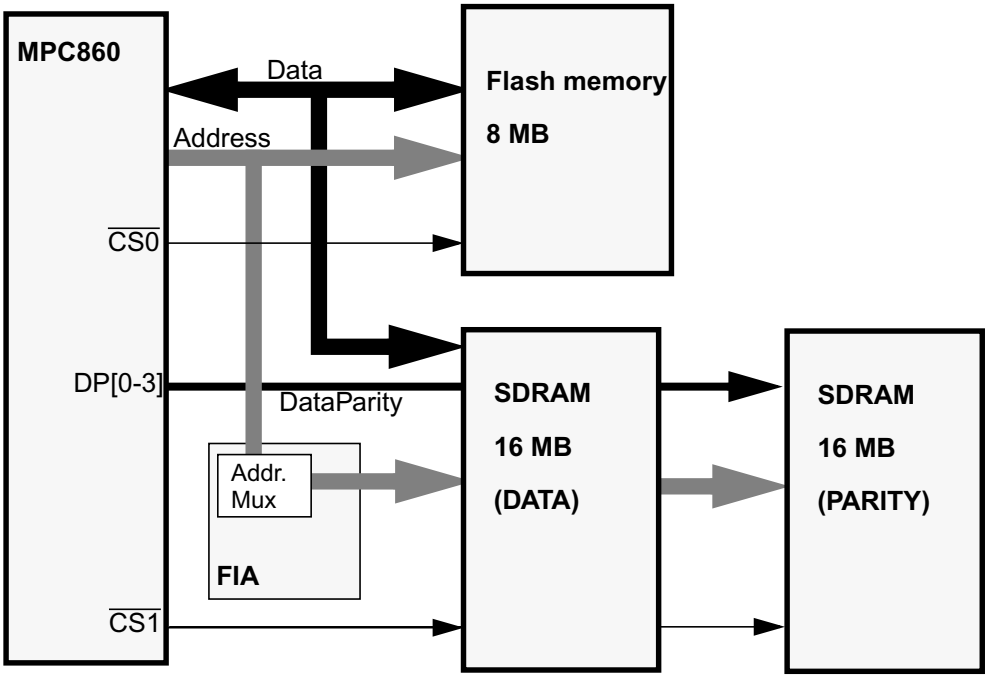


Figure 4: Interconnection between MPC860 and Memory

Flash memory

Flash memory size will be 8 megabyte at all. Two of Intels Advanced+ Boot Block Flash memories with a size of 32Mbit (each)will be used. These devices operates at 3.3V and can be read, write and erased at this voltage. The Flash memory is relatively fast and can support Boot-system and Flash file system. No parity supervision is done during Flash accesses.

The Flash memory devices are connected to the MPC860 as shown in figure 5.

The Flash memory contains all program code for both operating system and application software. Before executing programs the code is copied to the SDRAM. In addition to the programs a number of parameters is stored in the Flashes. These parameters describe the configuration of the hardware module and also the identification of the hardware module. The reason for this is to inform the OS which hardware configuration it is running on.
The Flash memory can be updated on board for easy software change.

After hard reset the system will boot from the Flash memory. The FIA drives a hard reset configuration word onto the system data bus. This will set the Boot Port Size to 32 bits.The MPC860 samples this word during reset.

The Flashes will be on-board programmed in production. JTAG is used to load the PBOOT part and Ethernet is used to load the OS.

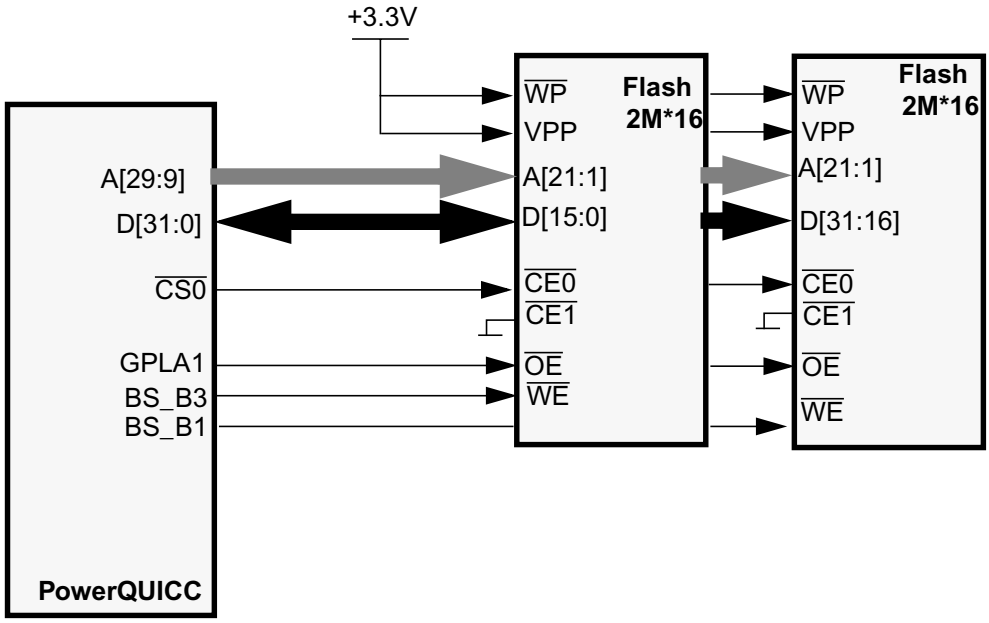


Figure 5: Interconnection between MPC860 and Flashes

SDRAM

32 megabytes of synchronous DRAM is used on SCB-RP. 16 megabytes (4Banks x 1M x 32bit) will be used by software, both for program and data storage. The other half will be used for parity storage.

When addressing a SDRAM two address accesses on the same pins are used, one row- and one column address access. Normally the MPC860 supports this addressing by using an internal address mux on its address bus. However, when the MPC860 shares the system memory with an external master (FIA can also be a master) this built-in address mux can not be used. The address needs to be muxed outside the MPC860, while control signals and the data bus are connected directly to the SDRAMs. The address multiplexing is implemented in FIA and is controlled with one of the UPM controlled general purpose lines of the MPC860. The main task of the address mux is to generate a row and a column address to the SDRAM. The mux implementation in FIA must be as fast as possible since it affects the access time to the system memory, and therefore there is no reclocking of the address done.The address delay through FIA is estimated to 15 to 20 ns. This timing will be enough to handle 6-1-1-1 read burst and 5-1-1-1 write bursts with good margins, see figure 6.

The memory address multiplexer in FIA only supports 32 bit data bus width, i.e the least significant bit on the column address is always A[29]. The width of the column address can be programmed to be eight or nine bits wide. The tables below shows the multiplexing function for both eight and nine bit column address.
On SCB-RP SDRAMs with 8-bit column address are used. Therefore multiplexing scheme shown in table 1 is used.

	MA[14]	MA[13]	MA[12]	MA[11]	MA[10][a]	MA[9]	MA[8]	MA[7]	MA[6]	MA[5]	MA[4]	MA[3]	MA[2]	MA[1]	MA[0]
ROW	A[7]	A[8]	A[9]	A[10]	A[11]	A[12]	A[13]	A[14]	A[15]	A[16]	A[17]	A[18]	A[19]	A[20]	A[21]
COLUMN	1 [b]	1 [c]	1 [c]	1	**precharge mode**	1	1	A[22]	A[23]	A[24]	A[25]	A[26]	A[27]	A[28]	A[29]

Table 1: Address mux when using eight bit column address

[a] This signal is *not* connected to any output pad of FIA. This address/ precharge bit is connected directly from the MPC860.

[b] This signal is not connected to the SDRAM.

[c] Instead of this signal A[8] and A[9] are connected directly from the MPC860. Since it is used as bank address.

	MA[14]	MA[13]	MA[12]	MA[11]	MA[10][a]	MA[9]	MA[8]	MA[7]	MA[6]	MA[5]	MA[4]	MA[3]	MA[2]	MA[1]	MA[0]
ROW	A[6]	A[7]	A[8]	A[9]	A[10]	A[11]	A[12]	A[13]	A[14]	A[15]	A[16]	A[17]	A[18]	A[19]	A[20]
COLUMN	1	1	1	1	**precharge mode**	1	A[21]	A[22]	A[23]	A[24]	A[25]	A[26]	A[27]	A[28]	A[29]

Table 2: Address mux when using nine bit column address

[a] This signal is *not* connected to any output pad of FIA. This address/ precharge bit is connected directly from the MPC860.

The memory controller provides four parity lines (DP[3:0]), one for each data byte on the PowerQUICC system bus. The parity on the bus is only checked if the memory bank accessed in the current transaction has parity enabled. The OS can enable parity checking/generation for a specific memory bank in the base register. The type of parity is defined in the SIUMCR register. Also, system protection is provided by defining each memory bank as read-only or read/write.

Parity can be configured for any bank, if it is preferred. Parity is generated and checked on a per-byte basis using PRTY[0:3], for the bank if the PARE bit is set in the BR register. The OPAR bit determines the type of parity (odd or even). Wether even or odd parity is used needs to be specified by SW.
Any parity error results in the assertion of the associated PERx bit in the MSTAT register and interrupt generation. See more about the parity control in the PowerQUICC Users's manual, reference /12/.

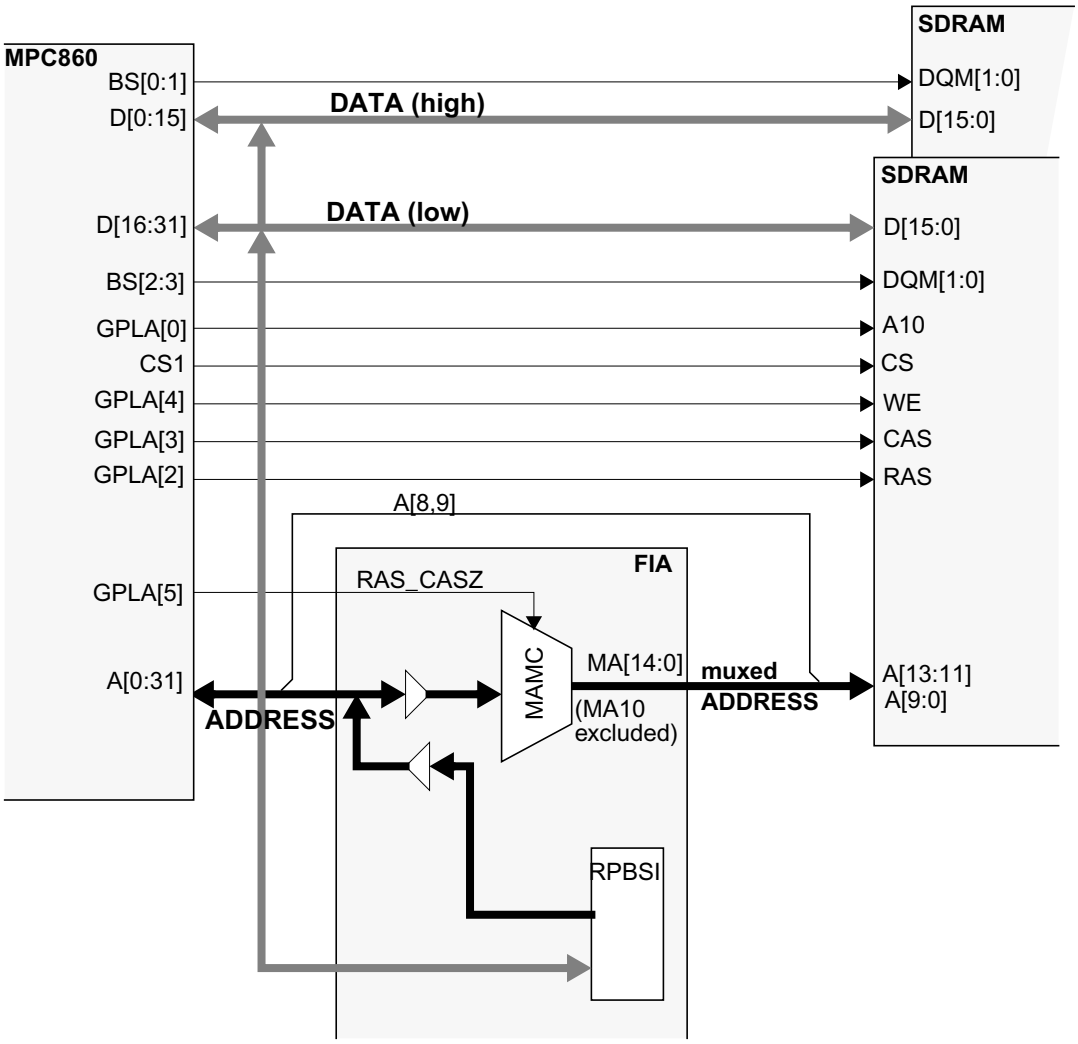


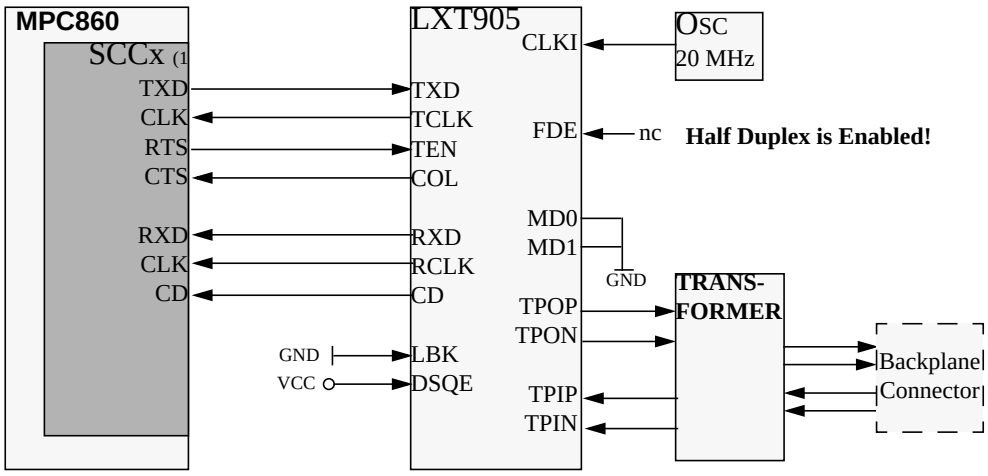
Figure 6: Interconnection between the MPC860, FIA and SDRAMs

4.1.2.4 Ethernet

The RPIHW1A provides two standard 10Base-T Ethernet connections.

The MPC860 provides the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. The two Ethernet ports of the RPIHW1A hardware module are implemented in SCC2 and SCC3 of the MPC860. Note that, when using SCC3 for ethernet SMC1 is not available due to memory conflict in the MPC860. The maximum bit rate on both ports is limited to 10 Mbit/s. Both ports support full duplex.

The MPC860 ethernet controllers interfacing glueless to a physical interface circuit. The transceiver chosen is the LEVELOne LXT905. The mode pins have to be tied to ground in order to set the LXT905 in MPC860-mode. Wether the Phy operates in half duplex or full duplex, can be determined by a hardware strapping pin (FDE). On SCB-RP (equal to RPIHW1A) half duplex is selected.
The impedance matching transformer will be a Bel Fuse S553-5999-86.



1) x=2,3

Figure 7: Ethernet implementation

4.1.2.5 Clock in RPI

A 40MHz system clock is generated by an oscillator and feed to the MPC860. The MPC860s CLKOUT signal is connected to a zero delay clock driver with integrated PLL. This device generates synchronous system clock towards FIA and SDRAMs and if used to devices connected to the ADB bus. The clocks are driven to each component separately. Some outputs of the clock driver are free and could be used by other devices.

The RPBSI block in FIA requires a 50 MHz clock. Determined by the signal *USE_EXT_CLK50* this clock can either be derived from the system clock (FIA internal) or can be taken from the *CLK50* pin directly (FIA external). FIA can handle system clock of either 40 MHz or 50 MHz. The signal *SYSCLK_IS_40* is used to inform FIA whether the system clock is 50 MHz or 40MHz. For the latter FIA will derive internally the 50MHz for RPBSI from the 40MHz clock.
On SCB-RP board the System clock is 40 MHz; FIA generates RPBSI clock internally from 40 MHz meaning the *CLK50* pin is not connected and *SYSCLK_IS_40* is tied to high.

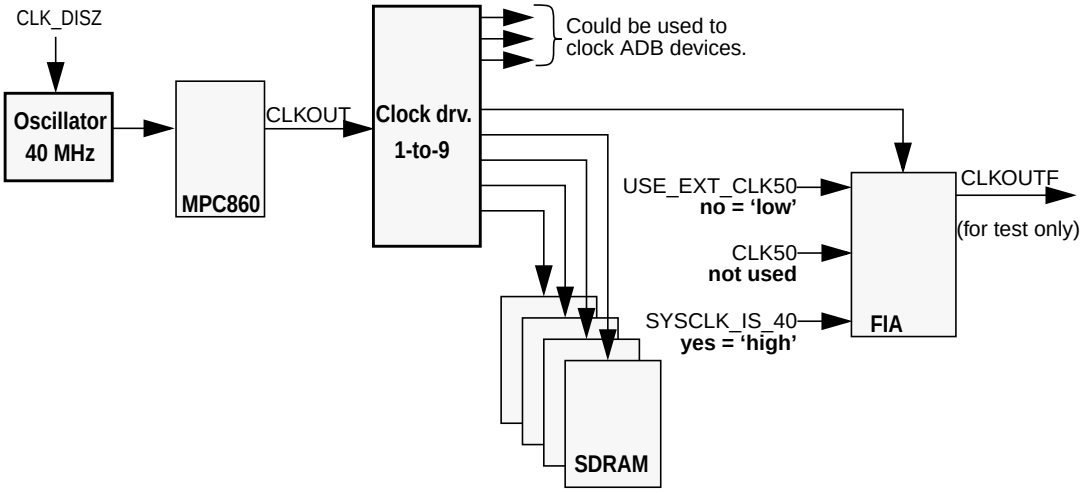


Figure 8: Clock distribution

4.1.2.6 Temperature Supervision

The RPI includes digital temperature sensors with I2C interface (LM75). The LM75 gives the possibility to read out the temperature at any time. In order to protect the PBA from damaging the LM75 features an overtemperature shutdown output. This output is connected to the power supply monitor in that way, that it generates a power on reset, in case that the temperature on the PBA exceeds a specific limit. This alarm threshold is either the default value (after power on = 80grdC) or a value programmed by the MPC860.

Additionally to this temperature sensor, which as part of the RPI is placed on the MB, there exist a second identical sensor on the DB. It is connected to the same I2C bus and can be addressed by a different address. Address for MB is '0'. Address for DB is '1'.

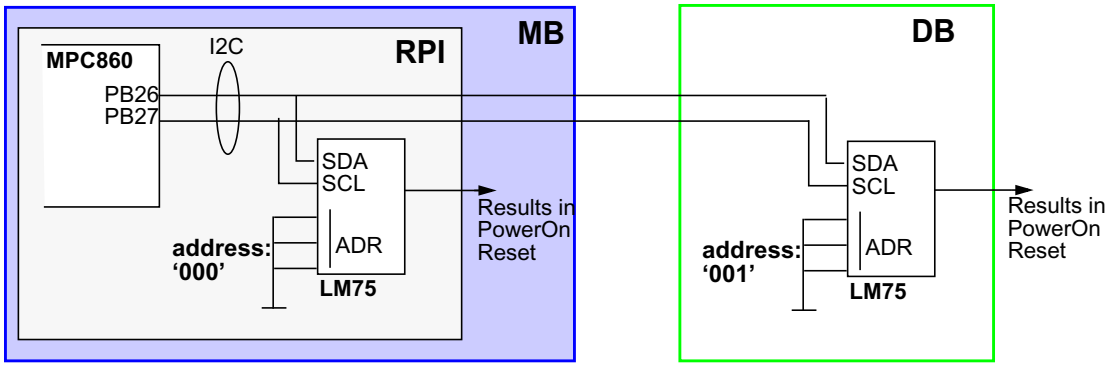


Figure 9: Temperature Supervision

4.1.2.7 Watchdog

The MPC860 includes a watchdog, which is used to generate a hard reset if it times out. The watchdog timer is enabled after hardware reset and is automatically set to the maximum time. The watchdog can then either be turned off or the time can be set. Once set the timer can not be changed and the watchdog cannot be turned off until the next reset.

4.1.2.8 Timers

The MPC860 includes the following timers:

- PIT:
  Periodic Interrupt Timer generates periodic interrupts for use with the real-time operating system. The PIT is clocked by the *pitrtclk* clock. The PIT function can be disabled if necessary.
- Power PC Decrementer:
  Power PC Decrementer is a 32-bit decrementing counter defined by the PowerPC architecture to provide a decrementer interrupt. This binary counter is clocked by same frequency as the timebase (also defined by the PowerPC architecture).
- RTC:
  The Real-Time Clock provides a time-of-day information to the operating system/application SW. It is composed of a 45-bit counter and an alarm register. A maskable interrupt is generated when the counter reaches the value programmed in the alarm register. The RTC is clocked by the *pitrtclk* clock.RTC can also be programmed to generate a maskable interrupt once each second.

4.1.2.9 Interrupts

Interrupts in RPIHW1A hardware module can be generated either internally or externally. Internal interrupts are generated from FIA or the MPC. External interrupts are generated from surrounding HW. The external interrupts can be used by the applications. They are connected to FIA.

The FIA is able to control interrupts from up to eight external sources. These external interrupts are available for the applications. The external interrupts are individually programmable for edge/level, low/high operation. The interrupts can be masked or unmasked in FIA.

Sources for FIA internal generated interrupts are RPBSI, Cicero Control and FIA main interrupt. Also the internal interrupts can be masked or unmasked by writing to the appropriate registers.

FIA can report three different interrupt causes to the CPU:
- FIA main reset
- RPBSI interrupt
- Cicero control interrupt

Note that RPBSI and Cicero control interrupt can also cause a FIA main interrupt if this is enabled.

The SIU (System Interface Unit) in the MPC860 controls MPC-internal and external interrupts coming from FIA.
The MPC internal interrupts are generated from sources like PIT, RTC, and CPM.
Additionally the signal *ADP_SRSTZ* (part of the ADP interface) is applied to the IRQ0 line of the MPC and generates an NMI to the MPC's core.

4.1.3 Power Distribution and Supervision

The SCB-RP board takes in -48V via two front connectors. The -48V is filtered and fed to the backplane seperatly in order to be distributed to all boards in the GEM magazine via XP03 to XP06. The magazine is divided in a left and a right half. So one -48V-branch supplies the left the other branch the right side of the subrack. The maximum power provided for each half is 400 Watts limited by the TSHOD (Two Step High Ohmic Distribution).

Since there exist two SCB-RP boards in a GEM the power supply is conveyed in two separate paths to each board (see figure 10).

The filter is supplemented by a discharging function. This circuit guarantees that the big capacitor of the filter are quickly discharged, when power supply is disconnected. This facilitates that a power failure can be detected immediately and that the big capacitors are already discharged when the board is pulled out of the subrack.

Power supervision is implemented for all -48V paths. In case of a power failure separate voltage alarms or A- and B-side and left and right GEM-half are generated towards the processor.

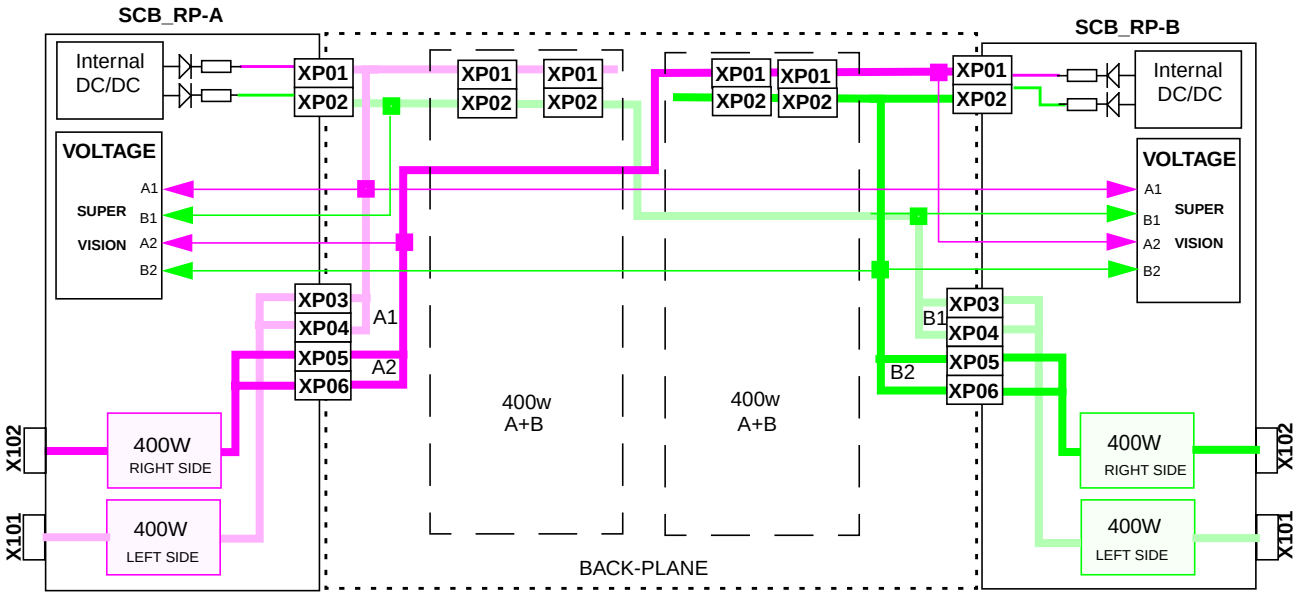


Figure 10: -48V distribution in GEM

Board power is supplied for SCB-RP from the backplane. The doubled -48V is connected together through protection diodes to the DC/DC converter.
The -48V will be converted to 3.3V, 2.5V, and 1.8V respectively.

Power supply monitor for all secondary voltage is included on the SCB-RP. The monitor is a LTC1326 device. It is connected to the power on reset input on the PowerQUICC. In case that any of the voltage drops below a specified threshold, the power reset is activated. This also forces drivers to the external world to be disabled.

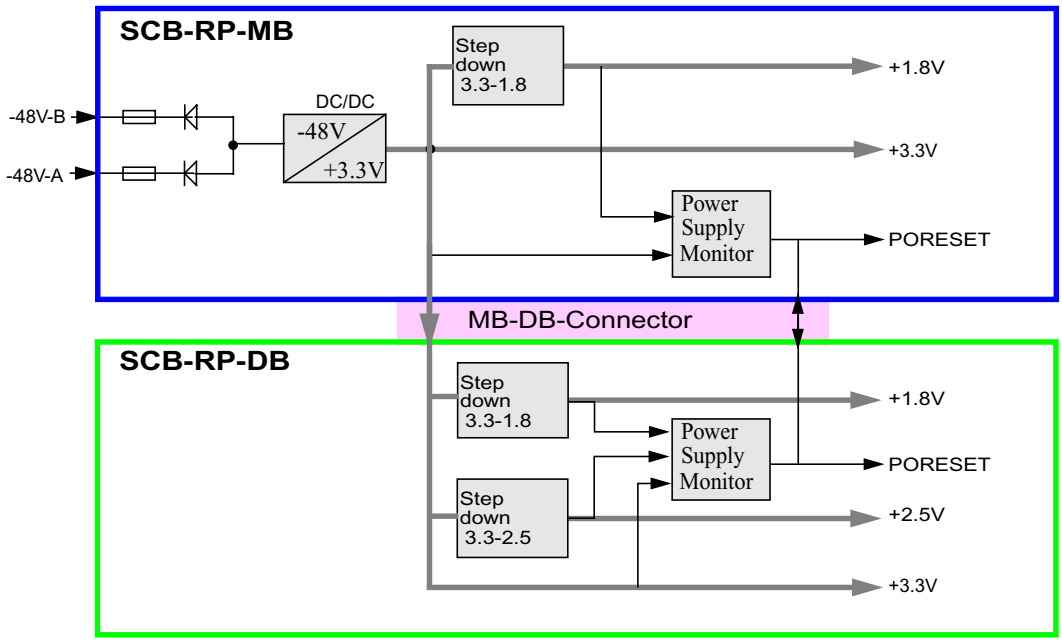


Figure 11: Power supply and voltage supervision

4.1.4 Reset

The main reset on the board is the power on reset (PORESTZ). This reset resets always all logic on MB and DB. This reset can be caused by:

- System power on.
- Overtemperature detection on MB or DB.
- Low voltage detection on either MB or DB of one of the secondary voltages.
- Sense of board insertion.
- ADP push button reset.
- PBIST reset.

Power on reset will also cause the hard reset signal (HRESETZ) and the soft reset signal (SRESETZ) to be activated. These signals have only effect on MB. The different reset levels and their effects are described below.

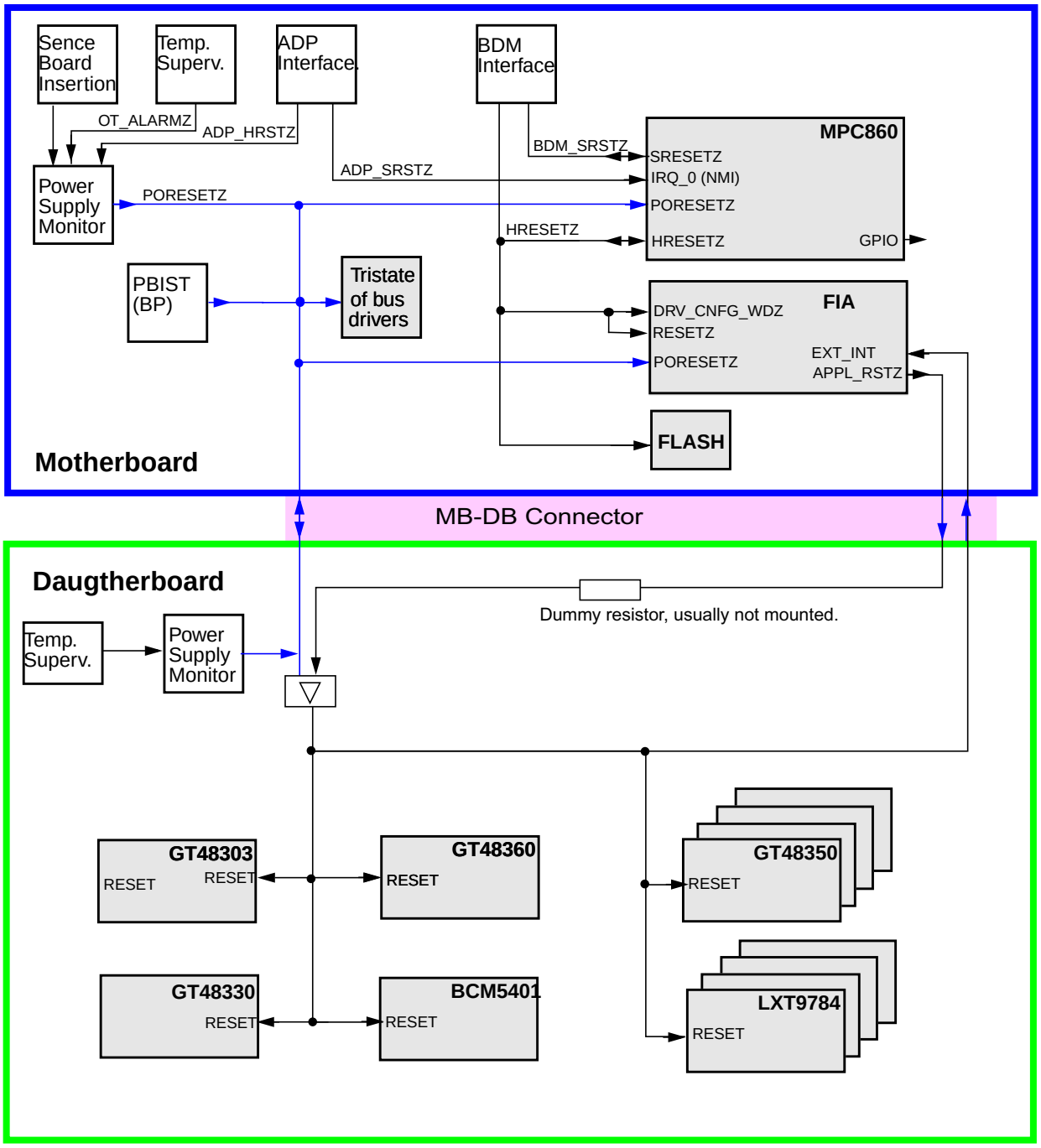


Figure 12: Reset logic

Different reset levels for MPC860 and FIA

1. Power-on reset

sources:
- power-on reset
- overtemperature alarm
- sense of board insertion
- ADP push button reset
- PBIST reset

effect on MPC860:
- reset of reset logic and PLL states
- reset of system configuration, clock module
- assertion of HRESETZ signal pin
- reset of debug port configuration
- reset of other internal logic
- assertion of SRESETZ signal pin
- sampling of hard reset configuration word

effect on FIA:
- reset of all logic including the application parts
- assertion of the application reset outputs
- during HRESET active, FIA drives the hard reset configuration word on the data bus towards MPC860

2. Hard reset

sources:
- external hard reset (HRESETZ signal pin)
- internal hard reset (PLL loss of lock, software watchdog reset, checkstop reset, debug port hard reset)
- cold-start by command (from software)

effect on MPC860:
- reset of system configuration, clock module
- assertion of HRESETZ signal pin
- reset of debug port configuration
- reset of other internal logic
- assertion of SRESETZ signal pin
- sampling of hard reset configuration word

effect on FIA:
- resets the RPI part of FIA
- there is no effect on the application part of FIA
- during HRESET active, FIA drives the hard reset configuration word on the data bus towards MPC860

3. Soft reset

sources:
- external soft reset (SRESETZ signal pin)
- internal soft reset (debug port soft reset)
- JTAG reset

effect:
- reset of debug port configuration

- reset of other internal logic
- assertion of SRESETZ signal pin

4.1.5 RPB-S

For communication with the CP, the SCB-RP provides a RPB-S interface.

RPB-S is connected to the SCB-RP via a front connector and distributed to the backplane. The front connection is of differential type while the connections towards the backplane are single ended.

Each RPI in the magazine is connected to two RPB-S/M branches, since there exist two SCB-RP boards in a GEM one handling path A (RPB-S/M-A) and the other path B (RPB-S/M-B).
The transmitters and receivers for A- and B-paths are all in separate packages to enhance fault-tolerance of the complete system, if one of them should break.

In order to reduce the load on the backplane bus, the RPB/M distribution is split into 4 branches, each handle up to seven boards. This is shown in figure 14.

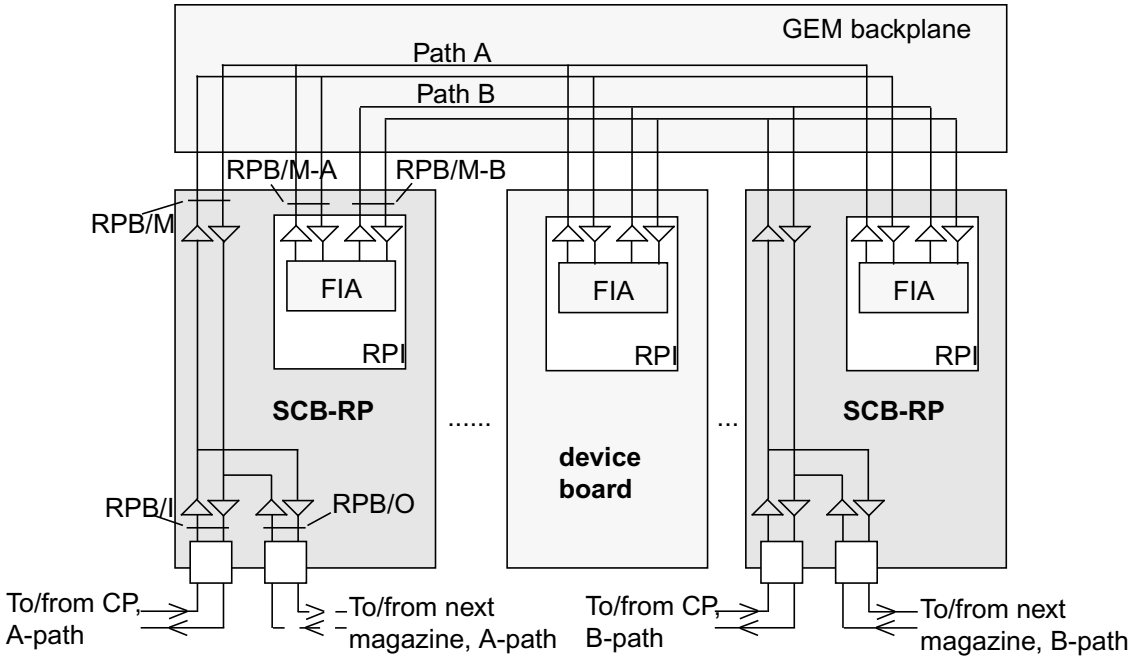


Figure 13: RPB-S distribution in GEM

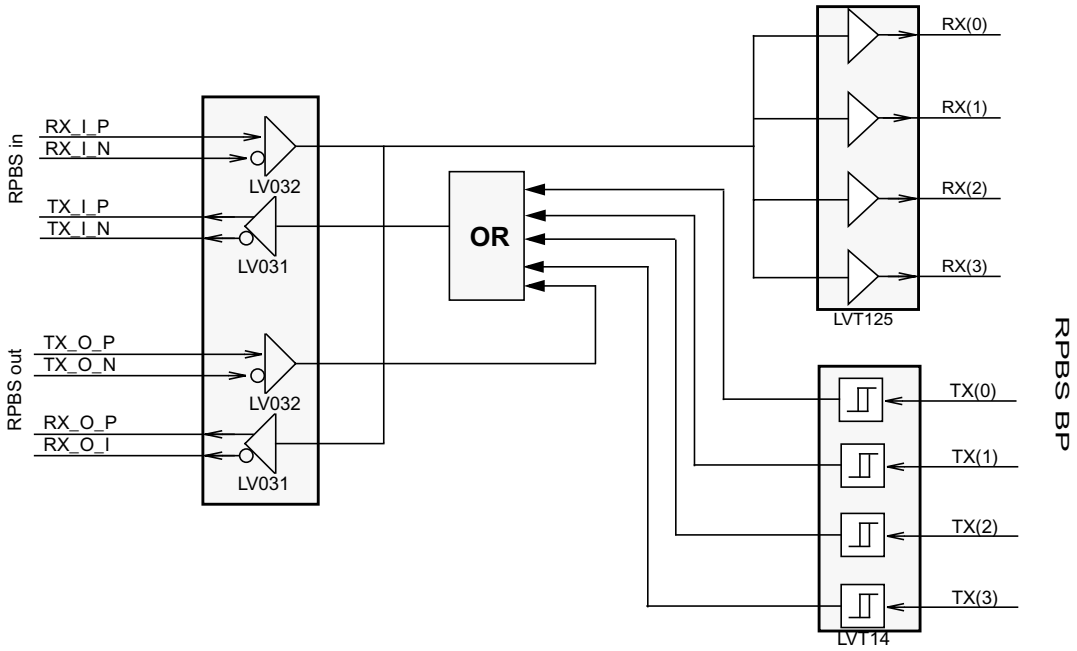


Figure 14: RPB-S transceiver block

4.1.6 V.24 Front interface

SCB-RP will provide a V.24 interface, which is accessible via a front connector. This is intended to be used for communication with a Fan magazine or a power distribution unit.

A Maxim RS-232 transceiver will be used to generate RS-232 electrical level. Only a subset of the RS-232 (CCITT V.24) specification is used i.e. no handshaking signals like RTS and CTS etc. are supported.
The SCC1 of the MPC860 is used as communication controller for the V.24 port.

Additional overvoltage protection is provided by a SMDA15 transient voltage suppressor.

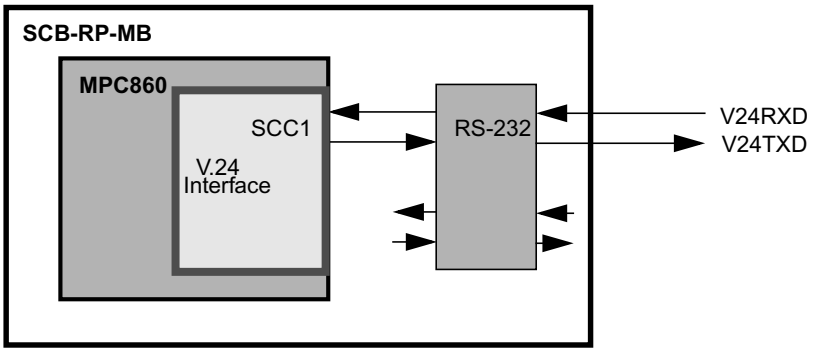


Figure 15: V.24 interface

4.1.7 External Alarm

SCB-RP will provide an interface for cabinet supervision. The intention of this interface is to improve the system's security within a cabinet. An alarm can be sent to the CP if the cabinet door is opened. The CP then can initiate actions to secure confidential data.

This interface is provided in a front connector on SCB-RP. The receiver circuit works as balanced interface. So the voltage between the wires A and B is decisive for the outgiven alarm signal. The alarm signal is connected to one of the processors GPIOs.
Protective diodes have been inserted to protect the circuits against too high and too rapid voltage peaks on the A and B wires. There is no hardware filtering of disturbances from a line, since these disturbances are filtered by the MPC860 SW.
The alarm sensors can be activated in two different ways, either by opening the A and B wires, or by closing or opening the B wire to the exchange earth 0V.
When an alarm sensor has changed alarm status, and kept its new status for a period longer than the filtering time indicated by the alarm system, the hardware sends an alarm message to the control system.

4.1.8 M-Bus

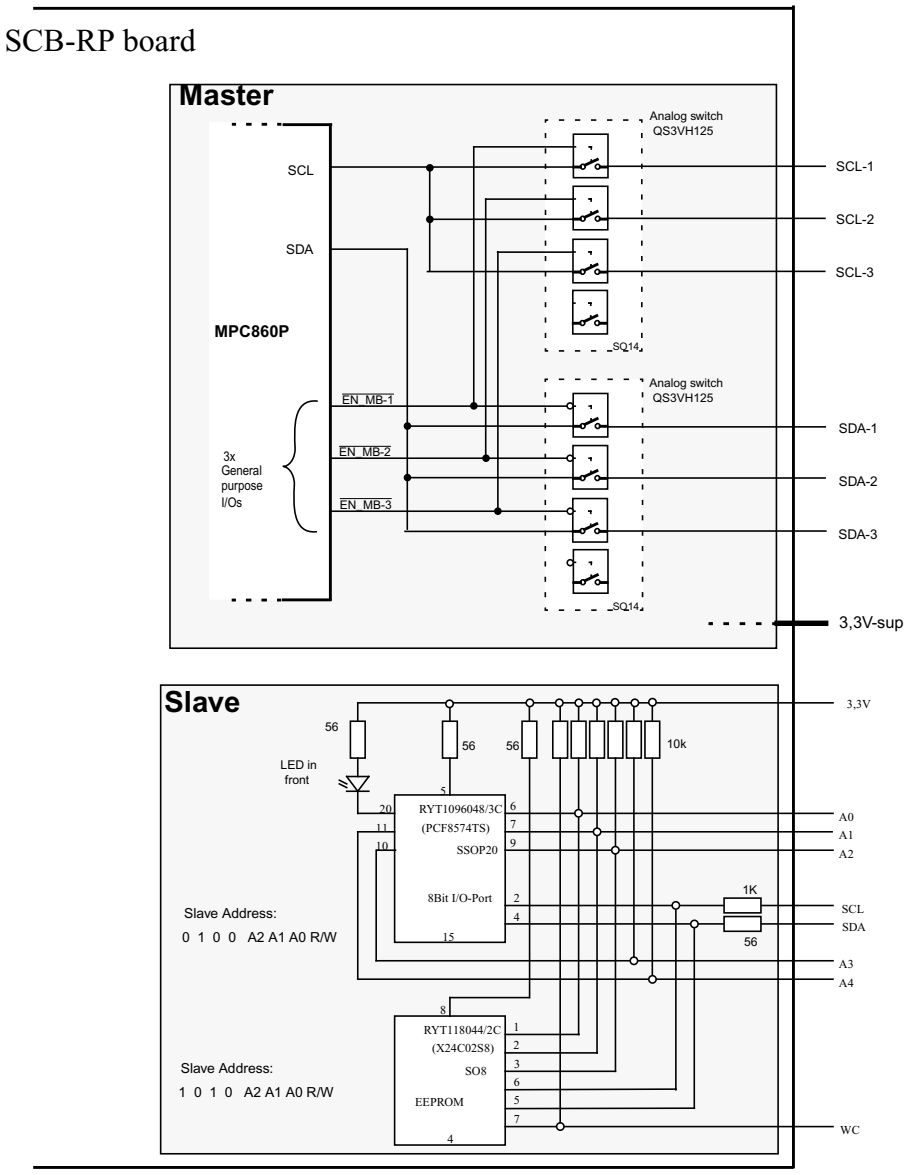
The SCB-RP provides the maintenance bus interface. This is implemented as a normal I2C bus. The SCB-RP board acts as the master on this bus, but has also a slave interface like all other boards in the GEM magazine.
The maintenance bus also gives the possibility to point out specific boards in a magazine by controlling the MIA-LED.

The M-Bus components on each board in GEM are powered and supervised by SCB-RP. Each SCB-RP board controls the M-bus slaves of the opposite half of the subrack including the opposite SCB-RP. The M-bus is not implemented with redundancy.

The M-bus address for for each slot is hardcoded in the backplane. An address pin connected to ground in the backplane = “0”. An open circuit address pin = “1”. Five address pins are used, which allow a maximum of 32 boards to be addressed. A0 is the least significant bit in the address.
Note: Slot address for physical addressing of the board and M-bus address do not use the same physical backplane pins, due to the separated power supply.

The used I2C devices can only handle three address bits. This means that one M-bus branch from SCB-RP can handle up to eight boards. Therefore the M-bus will be split into three branches so that the SCB-RP can handle up to 24 boards. The master must decide which branch has to be used to reach a certain board.

Figure 16: The Maintenance Bus interface



4.1.9 JTAG

In order to support programming, debugging and verification the SCB-RP provides a IEEE 1149.1 compatible JTAG interface towards the backplane. The JTAG interface is designed to allow access on board level (test fixture) as well as on subrack level (backplane bus). To support access to the JTAG port on subrack level a multidrop Addressable Scan Port (ASP) transceiver circuit (SN74LVT8996 from TI) is implemented. The board address is used for addressing. The ASP device needs to be placed close to backplane connector X01.

A JTAG tool can be connected to the subrack bus via address plug AP-2.

To guarantee signal quality for the JTAG backplane bus, termination is placed on SCB-RP board. This termination is connected via the backplane at the far end of the JTAG backplane bus only. See also table 17.

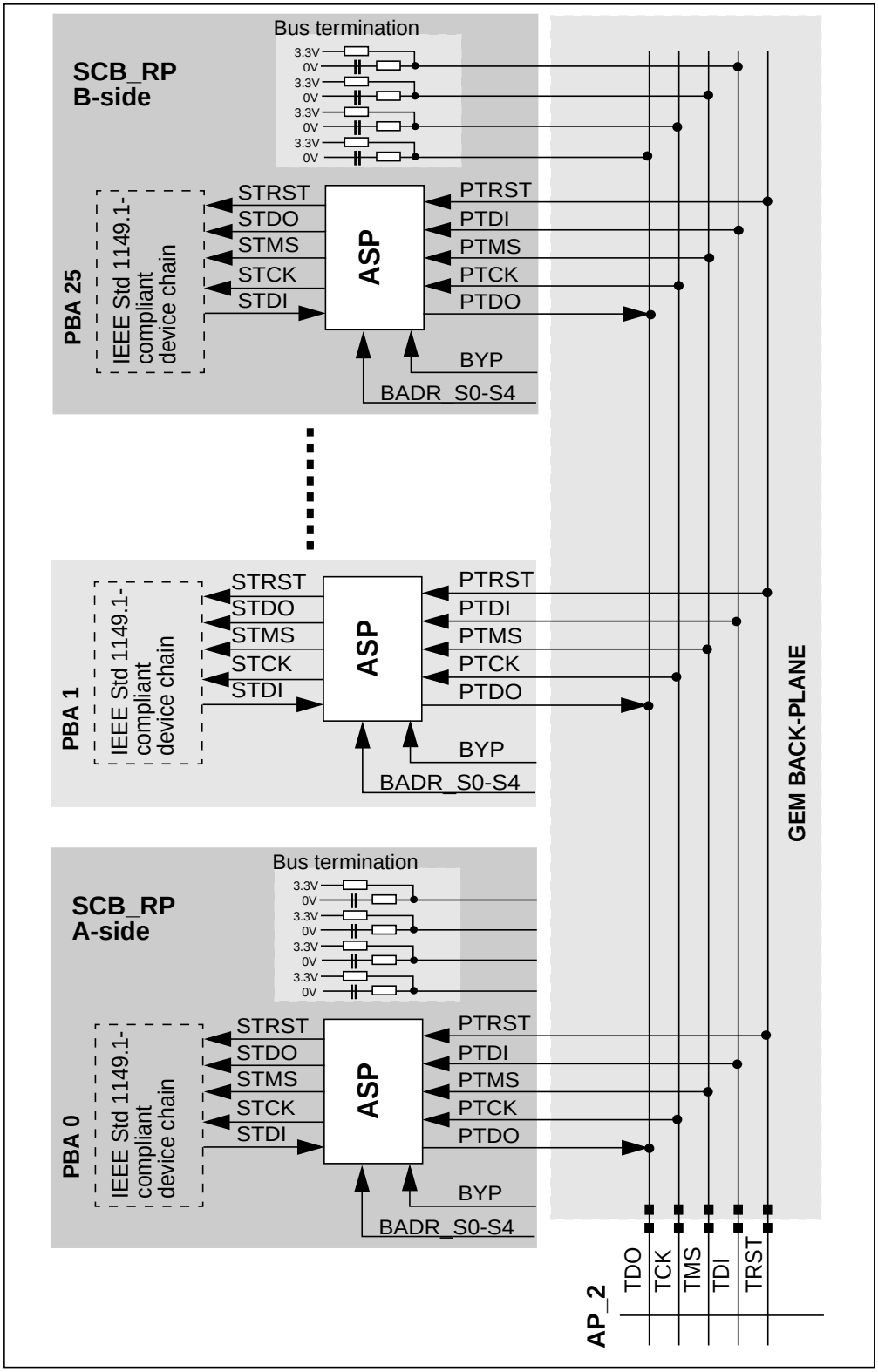


Figure 17: JTAG backplane connection

4.1.10 Ethernet Switch

Features:

- SCB-RP provides accessibility to all boards within the GEM via 10/100-BaseT Ethernet
- SCB-RP provides a 1000BaseT port and two 10/100 BaseT ports towards the front
- All Ethernet ports support autonegotiation, even the Gigagit port.
- All Ethernet ports support half or full duplex communication.
- The ports can be configured to support backpressure for half duplex.
- The switch provides automatic MAC address learning.
- The Ethernet switch support operation in managed and unmanaged mode.
- Flow control compliend to IEEE 803.x can be enabled.
- The switch can be configured for VLAN support.

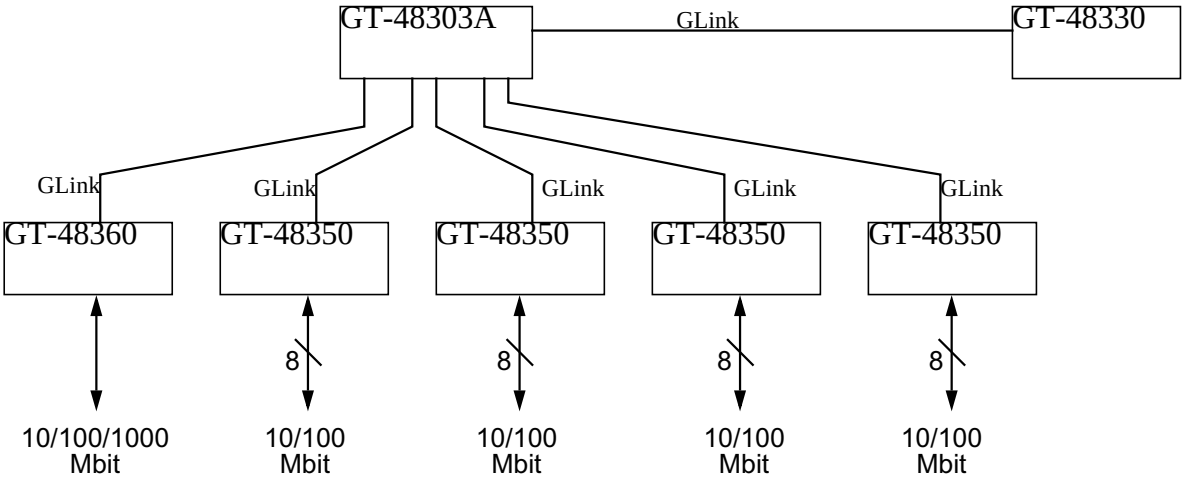
4.1.10.1 Switch Architecture

The Ethernet switch is build of a chip-set from Galileo Technologie, the so called GalNet Architecture. It is an extensible, scalable architecture for the switching of packetized data. All GalNet switching devices act as distributed intelligent agents within the switching system. Each switching device makes switching decisions independent of other devices in the system. This follows a distributed processing approach.

The Switch uses a ’store-and -forward’ approach, which allows switching between differing speed media (e.g. 100Base-TX and 10Base-T). The buffers required for ’store-and -forward’ are provided by on-chip RAM, that means no external RAM for storing packets and addresses is required.

The connection between the switching devices is done via the GLink bus. The GLink bus is a propritary generic bus for point-to-point connections. In order to connect more than 2 switching devices, a crossbar is used to switch GLink buses.

The architecture supports a maximum of 32 devices per system. Each devices (Ethernet switch or crossbar) needs to know about the existence of all other GalNet devices in the system in order to communicate information and packet data. The GLink crossbar switch also needs to know beyond which of its ports the other devices are located.



Note: Required Phy's and magnetics are not shown.

Figure 18: Architectural overview

4.1.10.2 Crossbar switch for G-LINK

The Crossbar switch' (GT-48303A) main function is to perform message routing between six GLink ports and a PCI port. (The PCI port is not used on SCB-RP board.) The GLink crossbar uses a non-blocking Crossbar architecture.

The GT-48303A does not store and forward, but rather relays the GalNet messages that the switch devices send to each other. Furthermore, the GalNet messages arriving on a GT-48303A port are likely to be multiplexed as Packet_Transfers between switches are multiplexed. The only latency that GalNet messages may experience in a GT-48303A is temporary congestion when multiple ports are targeting a single port within a GT-48303A.

Routing GLink messages is performed by looking up the target device number in the message header in the GT-48303A's Port Device Table registers and forwarding the message to be transmitted to the correct outbound port. The Port Device Table covers information about the devices connected to a specific port of the crossbar.

The GT-48303A supports an optional EEPROM interface for loading initial register values after Reset and during Normal operation. The supported EEPROM devices are 1K/4K/16K bit (x16 bit) with MicroWire interface. On SCB-RP the EEPROM is used to program the switching devices (GT-48350 and GT-48360).

4.1.10.3 Fast Ethernet block

The Fast Ethernet switching block is comprised of four 8 port switches. That makes a total of 32 Fast Ethernet ports. On SCB-RP only 28 ports are used, 2 towards the front and 26 towards the backplane. All ports are compliant with IEEE 802.3 standard and work either in 10Base-T or 100Base-TX mode, depending on autonegotion result.

One 8-port switch consists of a switching device with 8 MACs included, a 8-port Phy device and two quad magnetics.

The 8 port switches communicate with each other and with the rest of the system (Gigabit and Management CPU) via the GLink.

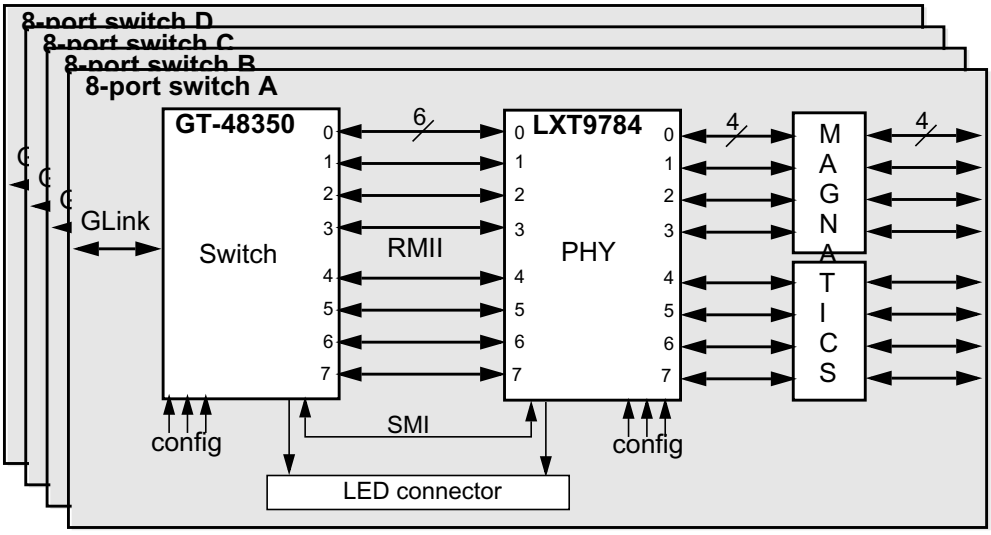


Figure 19: Fast Ethernet switch

10/100 MBit 8-port switch - GT-48350

The main function of the GT-48350 is to switch between eight 10/100Mbit Ethernet Reduced Media Independant Interface (RMII) ports and the GLINK bus. The device includes the MAC function and LED interfaces. All system memory is on-chip, therefore there are no external data and address DRAMs.
The GT-48350 integrates 160 packet buffers for Data. 128 are shared by the ports and 32 are dedicated for the GLink. The address table size is 8k supporting learning of 3.5K addresses.

The GT-48350 interfaces with the LXT9784 via the RMII and the SMI. The RMII is compatible to the rev. 1.2 specification of the RMII consortium.

The GT-48350 supports following features:

- Flow control support on any full duplex port.
  Flow control is the process of controlling data transmission at the sender to avoid overfilling buffers and loss of data at the receiver. The GT-48350 supports IEEE 802.3xx flow control by using the pause operation, when operating in full duplex. The GT-48350 will avoid transmitting new packets for a specific time, after it received a pause packet. It also sends a pause packet after the number of packets in the receive buffer exceeds a programmable threshold.

- Backpressure algorithm on any half duplex port.
  Backpressure is the process of controlling data transmission at the sender to avoid overfilling receive buffers and loss of data at the receiver. The GT-48350 enters backpressure mode when the number of packets in the receive buffer exceeds a programmable threshold.

- Autonegotiation between 10/100 MBit/s.
  Algorithm that allows two devices at either end of the link to negotiate common data transmission parameters (e.g. transmission rate, half vs. full duplex, etc.) in order to achieve the best possible mode of operation over a link.

- Address self-learning mechanism.
  This mechanism allows the switch devices to learn which station (address) is on which segment of the Ethernet network (i.e. on which port). This is done by looking at the source address in all of the frames the switch receives.

- Port trunking for increased bandwidth.

Port trunking provides for increased bandwidth between two Ethernet stations by by allowing multiple ‘physical’ links to be combined to operate as a single ‘logical’ link.

- Head-of-Line blocking prevention.
  Head-of-line blocking prevention is a mechanism which prevents packkets from being sent to a ‘blocking’ port. A port may become blocking when ‘too many’ packets are queued to this port. The concept adopts the approach that it is prefarable to discard packets to congested ports than to allow them to consume more and more buffers, as eventually other ports will become blocked too, due to a shared buffer pool.

Octal PHY - LXT9784

The LXT9784 is a single chip transeiver device containing eight independant 10/100 MBit transceiver with RMII interfaces.

The LXT9784 supports both autonegotiation and parallel detection. It also features an automatic MDI crossover function, thus eliminates the need of crossover cables. The integrated hardware integrity function detects and report cabling problems via the serial management interface.

Magnetics:

The magnetics have a 1:1 RX and TX ratio. They support both 10 and 100Mbit operation. Various vendors for these devices exist, for instand Belfuse and Pulse Engineering.

4.1.10.4 Gigabit Ethernet Block

Gigabit ethernet block consists of a switching device (GT-48360) with a MAC included, a Gigabit-Phy device (BCM5401) and a transformer.

The Gigabit port is compliant with IEEE 802.3 standard and work either in 10Base-T, 100Base-TX or 1000Base-T mode, depending on autonegotion result.

The Gigabit switch communicates with the rest of the system (Fast Ethernet and Management CPU) via the GLink.

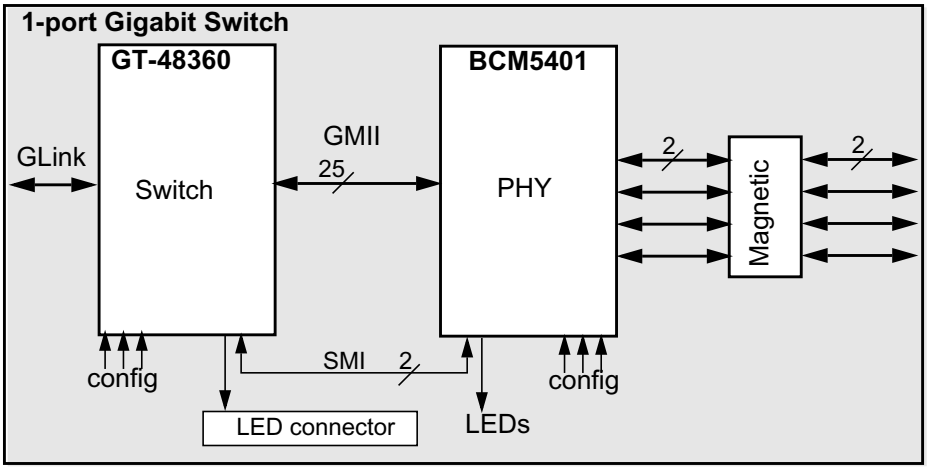


Figure 20: Gigabit Ethernet switch

Gigabit switch - GT-48360

The main function of the GT-48360 is to provide packet switching function between one on-chip 10/100/1000 Ethernet port and the GLINK bus. The integrated MAC function supports all three speeds. All system memory is on-chip, therefore there are no external data and address DRAMs.
The GT-48360 integrates 80 packet buffers for data with programmable sharing scheme. The internal address table supports learning of up to 8k addresses.

The GT-48360 interfaces with the Gigabit Phy via the MII or GMII depending on the speed and the SMI. MII and GMII are compliant to the IEEE 802.3 specification.

The GT-48360 supports following features:

- Flow control support in full duplex mode.
- Autonegotiation between 10/100/1000 MBit/s
- Address self-learning mechanism.
- Port trunking for increased bandwidth.
- Head-of-Line blocking prevention.

Gigabit PHY - BCM5401

The BCM5401 is a single chip device that performs all the physical layer interface functions for 1000Base-T and 100BaseTx, and 10BaseT Ethernet on CAT 5 UTP cable. The device performs allencoding, decoding, data recovery clock recovery, stream cipher, digital adaptive equalization, echo cancellation, line transmission, line integrity functions and management functions.

The BCM5401 is fully compliant with the IEEE 802.3 standard.

The BCM5401 supports auto - negotiation between all three speeds according to IEEE 802.3u and 802.3ab specifications. Auto - negotiation can be enabled and disabled by hardware or software. On SCB-RP board it is enabled by hardware, but can be disabled by software.
The BCM5401also features an automatic MDI crossover function, which means that RX - TX swaps are corrected for 10/100 Mbit operation. This eliminates the need of crossover cables.
During 1000BaseT operation, the BCM5401 has the ability to automatically detect and correct some cable wiring errors. This includes polarity errors caused by swapping of wires in a pair as well as swapped pairs. During 10/100 operation, pair swaps are corrected.

Magnetics:

The implementation of triple speed operation requires the use of a simple magnetic containing four 1:1 isolation transformers with built-in common mode chokes.

4.1.10.5 Ethernet Management Support

Via the Ethernet Management interface the CPU on the MB have read write access to the Ethernet switch. This allows following functions to be supported:

- (Re-)Configuration of the Ethernet switch
- Collecting of network statistics
- VLAN support
- Port monitoring (Sniffer function)

- Spanning tree support

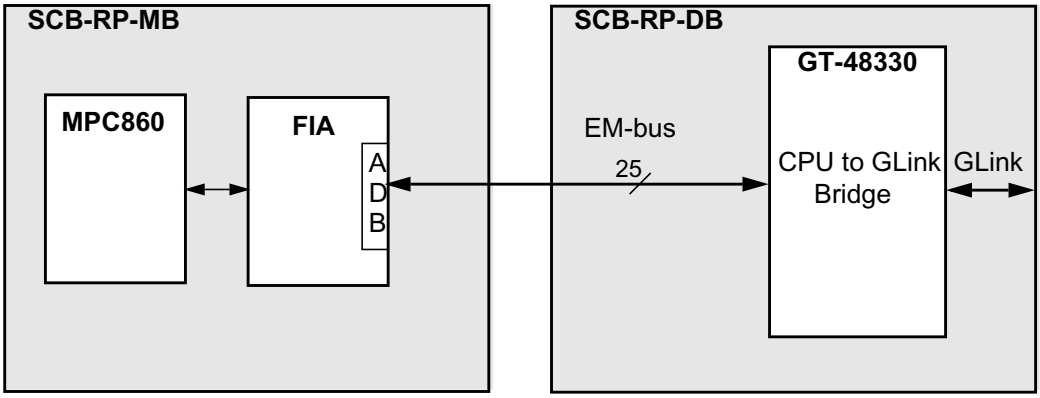


Figure 21: Ethernet management

CPU-to-GLink bridge - GT-48330

The GT-48330 provides a simple hardware interface from FIAs ADB bus to the GLink bus.It transforms CPU reads/writes into GLink messages. The capability is used to read/write registers in the switching devices.
The GT-48330 provides on-chip packet buffering for packets forwarded to the CPU. It also supports packets forwarded by the CPU for instance SNMP trap messages. It provides an on-chip interrupt controller for interrupt messages received from the switching devices.

4.1.10.6 Clock Distribution for Ethernet devices

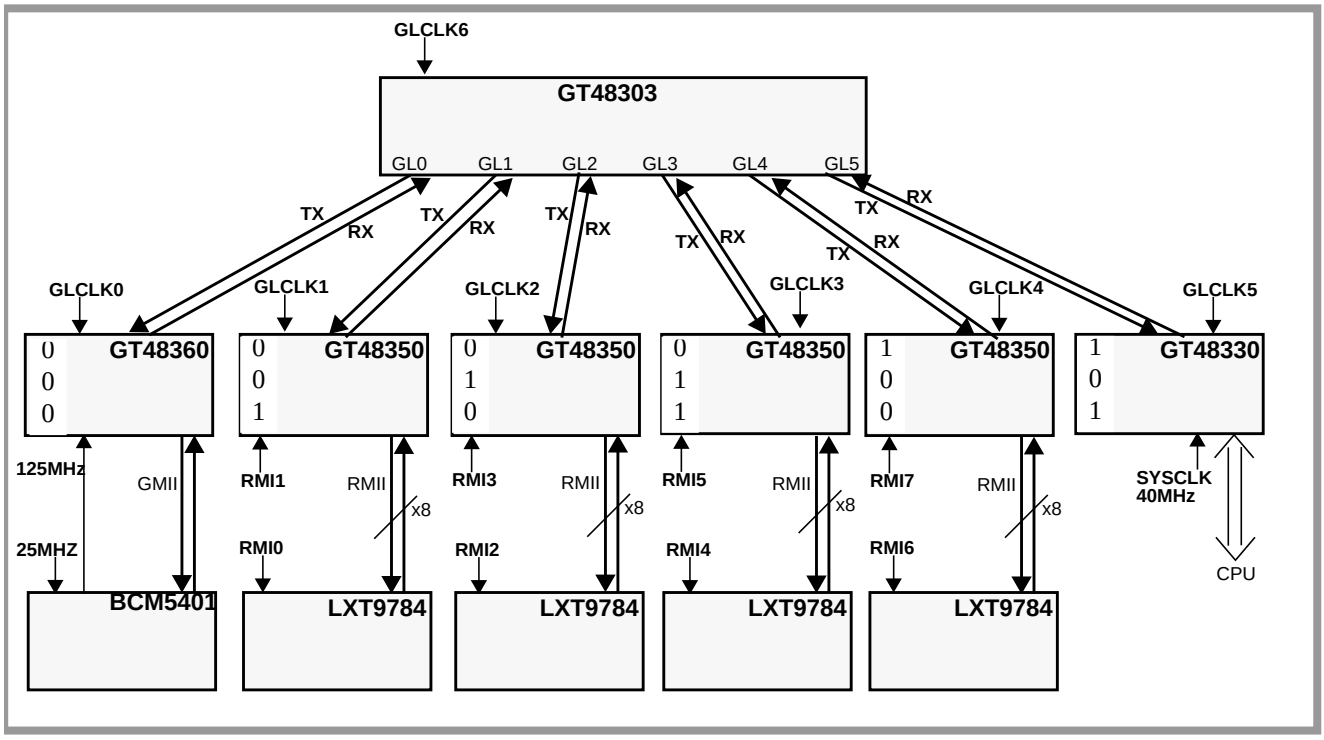


Figure 22: Clocks and interfaces

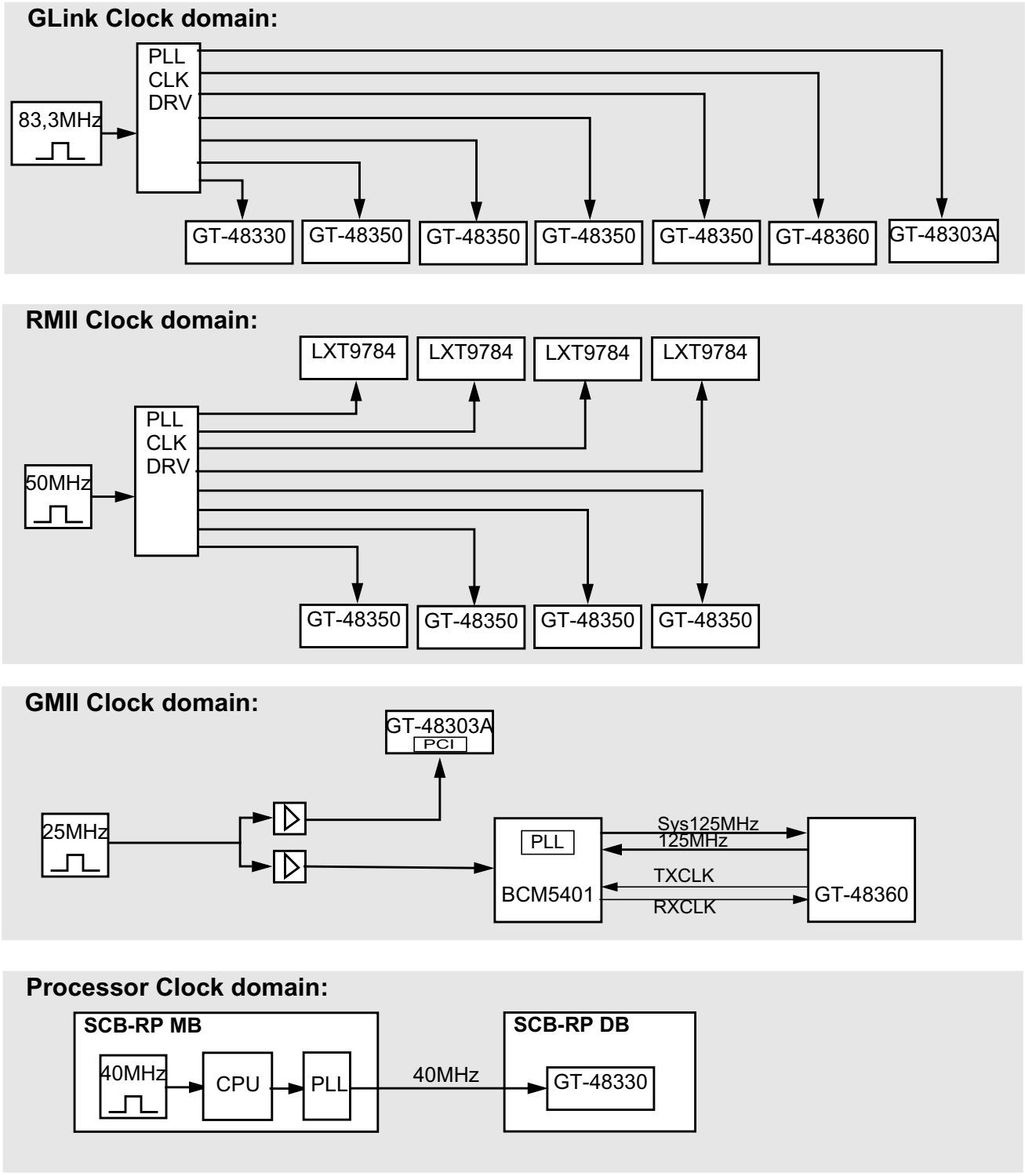


Figure 23: Clock domains of the Ethernet switch

4.1.10.7 Initialization and Programming of the Switch' Configuration

Several alternatives are supported for initialization and configuration of the Ethernet switch.

- **Strapping pins:** The switch devices read the configuration from strapping pins during reset. By help of the strapping pins only a few basic settings like device number, number of devices, SMI mode and so on can be done.
  On SCB-RP the strapping pins are set in that way, that the Ethernet switch can start operation, even if no EEPROM or CPU is connected.

- **Configuration EEPROM:** Configuration via EEPROM is a more sophisticated configuration method. All internal configuration registers of the switch devices, the crossbar and the Phy devices can be accessed. This allows optimal configuration of an unmanged switch with regard to the systems requirements.
  On SCB-RP one EEPROM is attached to the Crossbar switch. All registers within the GT-48303A can be directly addressed. Registers in other devices attached to the GT-48303A can be indirectly addressed by writing a specific register in the GT-48303A. When written to this specific register the GT-48303A will automatically generate a GLink message towards the addressed device (see figure 24). The configuration file stored to the EEPROM is CXC.

- **Configuration via Management CPU:** In a managed switch the CPU can setup the complete switch configuration by writing to appropriate configuration registers in the switch devices. The configuration can be changed during operation if necessary.

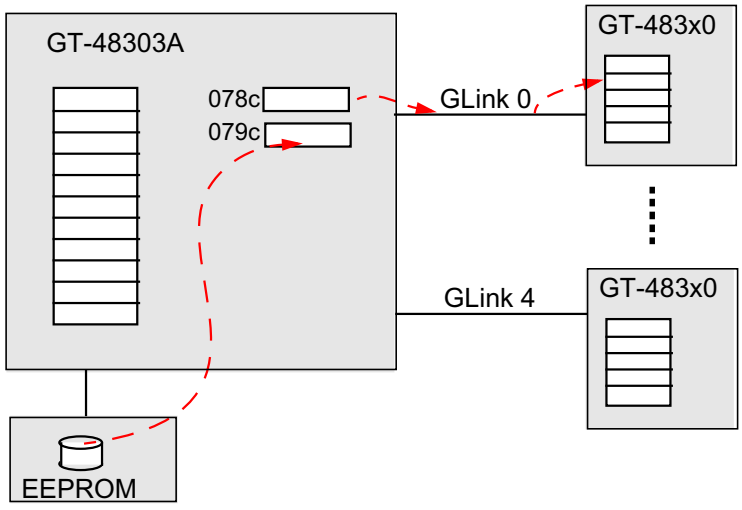


Figure 24: Configuration of the Ethernet Switch from EEPROM

Note: As already mentioned, the Ethernet switch on SCB-RP can be configured to operate in different modes. This document does **not** describe the actual settings made in the switch. It only describes settings made in hardware. But those can be overwritten be EEPROM content or from CPU. So, please refer to the actual configuration file, which is going to be stored to the EEPROM. Or check the Ethernet Management software modules, if there are any.

4.1.10.8 Ethernet Cabling

The SCB-RP Ethernet interfaces are designed to connect to a remote Ethernet station by using a plain one-to-one cable. This means the crossover function is implemented on the SCB-RP board. The signal names on the SCB board however refer to the internal circuits on SCB-RP not to the station in the other end.

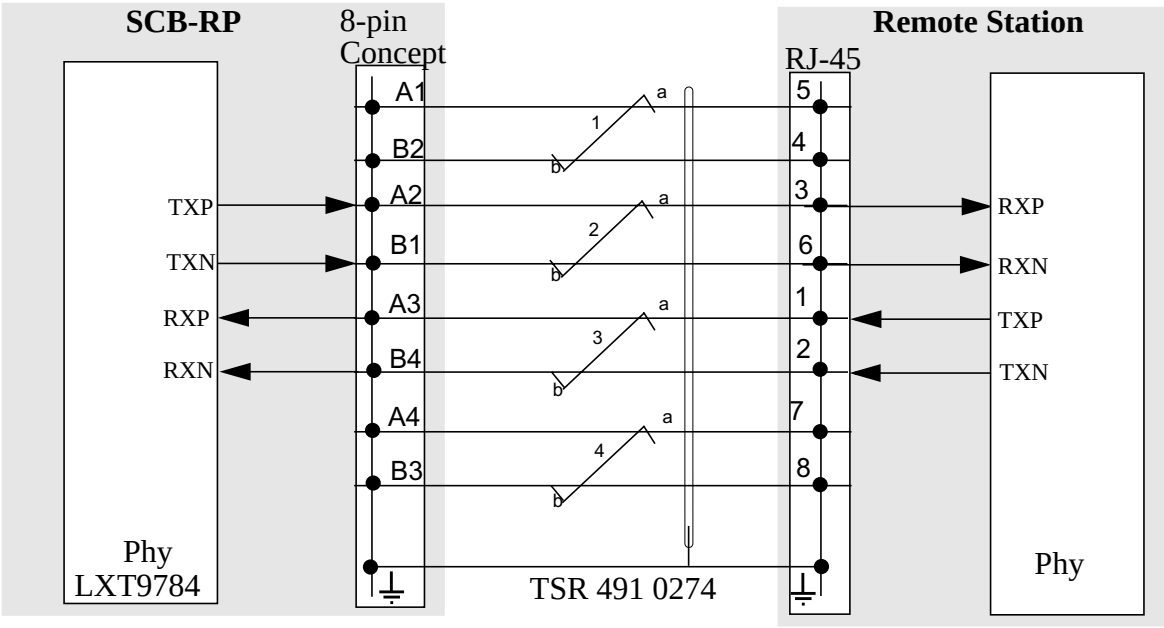


Figure 25: Ethernet connection scheme for 8-pin Concept connector

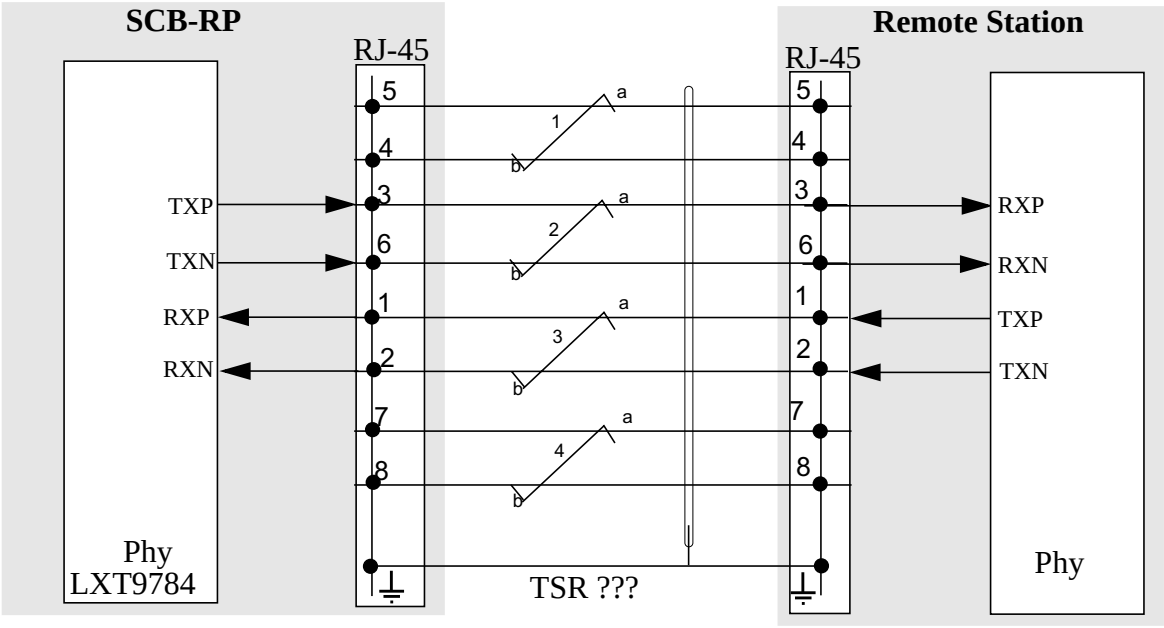
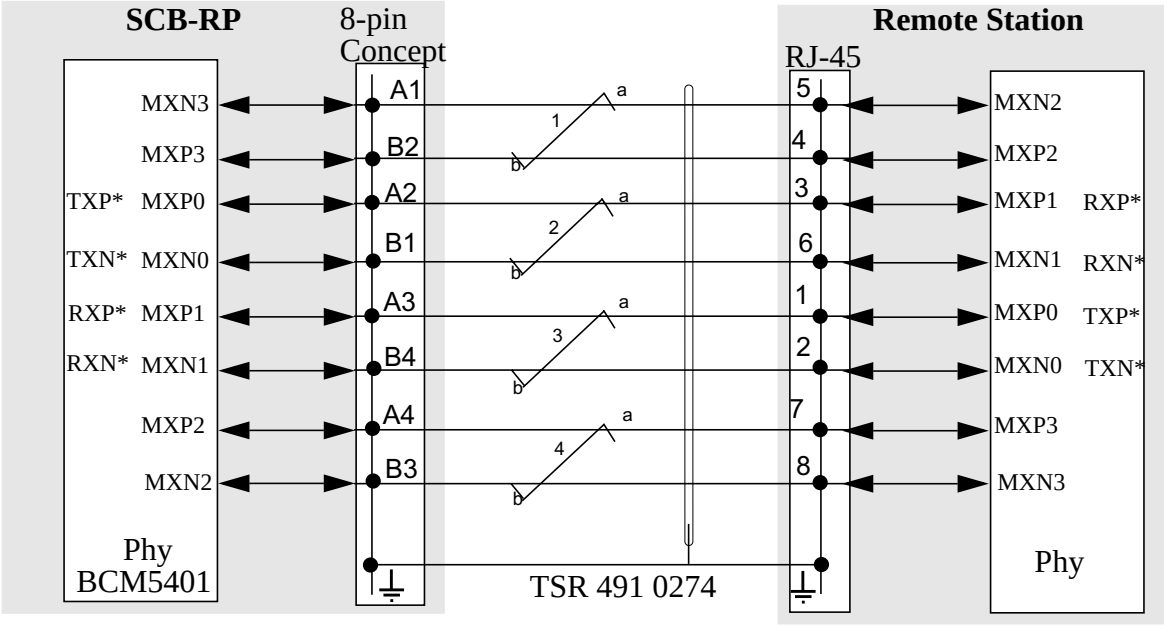


Figure 26: Ethernet connection scheme for RJ-45 connector



*) These names refer to the function of the pins, when the interface works in 10/100BaseT mode.

Figure 27: Gigabit Ethernet connection scheme for 8-pin Concept connector

4.2 Functional Modes

4.2.1 Production Test Mode

The production can do functional tests of the components of RPIHW1A hardware module with P-BIST controlled by the on-board processor. P-BIST is mainly used for memory tests (RAM and Flash), FIA processor interface test and read/write operation to certain locations.

For production testing the SCB-RP also provide a standarized JTAG interface. This interface allows connectivity tests between components as well as sampling and setting of chip I/Os.
In addition the JTAG interface is used by the production to load the boot and basic system programs into the Flash memory and can also be used to program the configuration EEPROM for the Ethernet switch.

4.2.2 Operational Modes

4.2.2.1 Start Up Operation

<u>MPC860 SPLL Power-on Reset Configuration:</u>

While the power on reset is active, the reset configuration of the SPLL of the MPC860 is sampled on the MODCK pins. On these pins the multiplication factor PLPRCR[MF] = ‘10’ is adjusted. Meaning the processor starts up with an internal frequency identical to the external oscillator frequency. Depending on the hard reset configuration word, the SCCR[EBDF] will be initialized to either ‘00’ or ‘01’ meaning the external bus will run at the internal frequency (full speed) or at the half speed respectively.

<u>Hard Reset Configuration:</u>

When hard reset is active, a hard reset configuration word is driven by the FIA ASIC onto the data bus. The MPC860 determines its initial mode of operation by sampling the values present on the data bus (D[0-31]) during hard reset active.
The hard reset configuration word driven by FIA is shown in table 3.

Table 3: Hard reset configuration word

Bits	Name	Value	Description
0	EARB	0	External ARBitration. Set to ‘0’ means internal bus arbitration is performed.
1	IIP	0Various vendors for these devices exist, for instand Belfuse and Pulse Engineering.	Initial Interrupt Prefix.
2		0	Reserved.
3	BDIS	0	Boot DISable. Is set to activate the memory controller so that it match all addresses.
4	BPS	0	Boot Port Size. Is set to 32-bit port size.
5		0	
6	-	0	Reserved.
7	ISB	1	Initial internal Space Base select.Defines the initial value of the IMMR bits 0-15 and determines the base address of the internal memory space.
8		0	
9	DBTGC	1	DeBuG pin Configuration. Configures the operation of a lot of signals (compare with “MPC860UM/AD Table 12.3”)
10		1	
11	DBPC	1	DeBug Port pins Configuration. Determines the active pins for the development port.
12		1	
13	EBDF	0	External bus division factor. 00 Full speed bus. (01 Half speed bus.)
14		0	
15	-	0	Reserved.

Soft Reset Configuration

The rising edge of the SRESETZ signal is used to configure the development port (BDM). Before SRESETZ goes inactive, DSCK is sampled to determine for debug-mode enable/disable. After SRESETZ is disasserted, if debug mode was enabled, DSCK is sampled again

for debug-mode entry/non-entry. DSDI is used to determine the debug port clock mode and is sampled after the negation of SRESETZ. The Soft Reset configuration is provided by the debug port controller.

4.3 Indications and Alarms

There is a MIA LED in the front of the SCB-RP, indicating that manual intervention is allowed when it lits.

The SCB-RP features an external alarm interface, which could be used to provide cabinet intrusion alarm.

4.4 Self Diagnostics

The operating system is executing power up diagnostics and self test after power up.

4.5 Control Functions

The RPI hardware module includes a temperature supervision circuitry. The used component, a LM75, is a temperature sensor and an over-temperature detector with I2C interface.On SCB-RP there is a second identical sensor circuit located on the DB. The MPC860 can query both sensors via the I2C interface at any time to read temperature.
The open drain overtemperature shutdown output (*OT_ALARMZ)* becomes active (low) when the temperature exceeds a programmable limit. The processor is able to program both the temperature alarm threshold and the temperature at which the alarm condition goes away (hysteresis).

The assertion of one of the sensors overtemperature alarm outputs, will result in a power on reset meaning both MB and DB are reset. The SCB-RP will be held in reset state until the temperature falls below the programmed threshold.

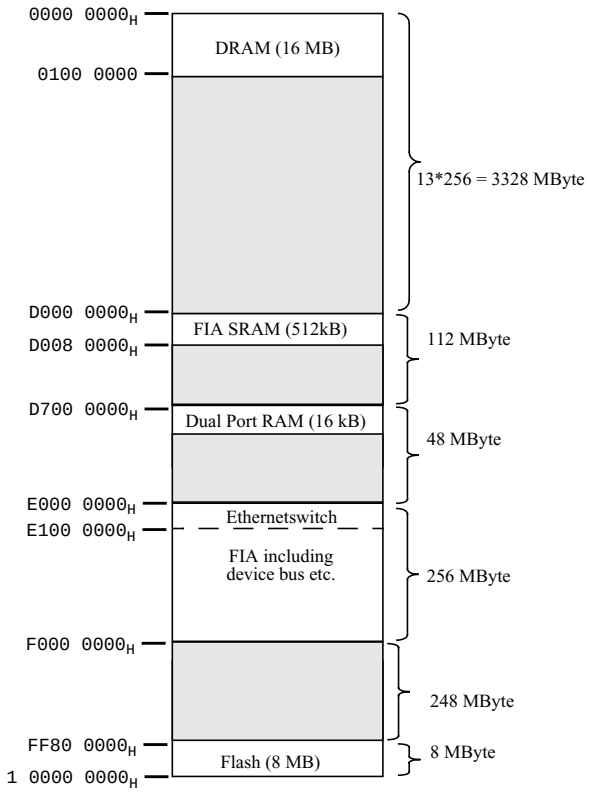
The thermostat settings for the board can be stored as parameters in the Flash. The OS can then read this values and program the thermostat registers after a power-on reset. If the OS does not program the thermostat, the default settings will be valid. This is 80grdC alarm activating and 75grdC deactivating (5grd hysteresis) temperature threshold.

Note: The overtemperature shutdown cannot be disabled by software!

4.6 Synchronisation

There is no external synchronisation of the SCB-RP necessary.

5 Memory map



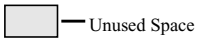


Figure 28: Memory map of the RPI

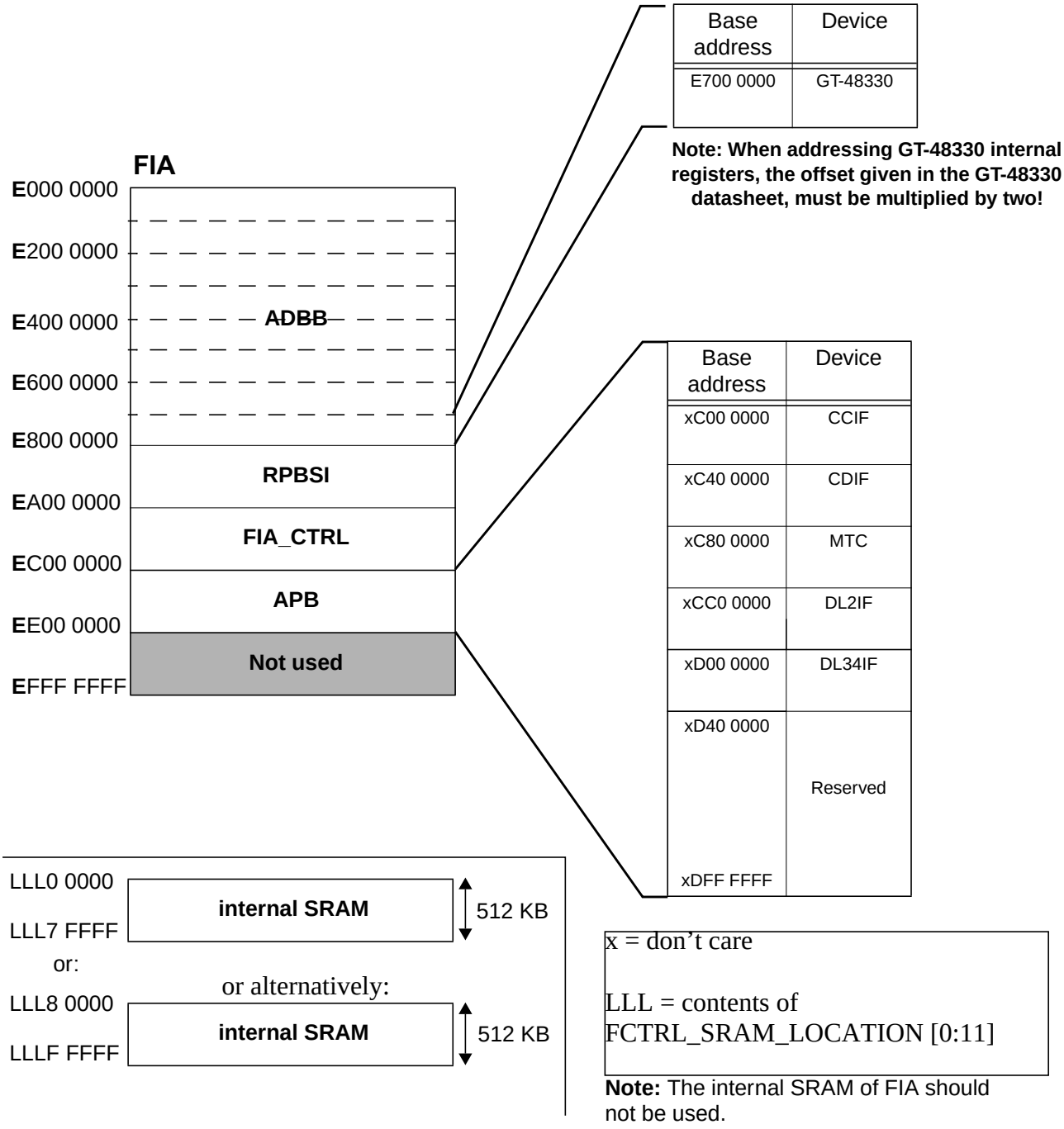


Figure 29: Register map of the FIA

For detailed register description of the specific devices refer to reference /3/ and reference /12/ to reference /18/.

6 Electrical Requirements

6.1 External Interfaces

The SCB-RP is interfacing with external interfaces.These interfaces are described below.

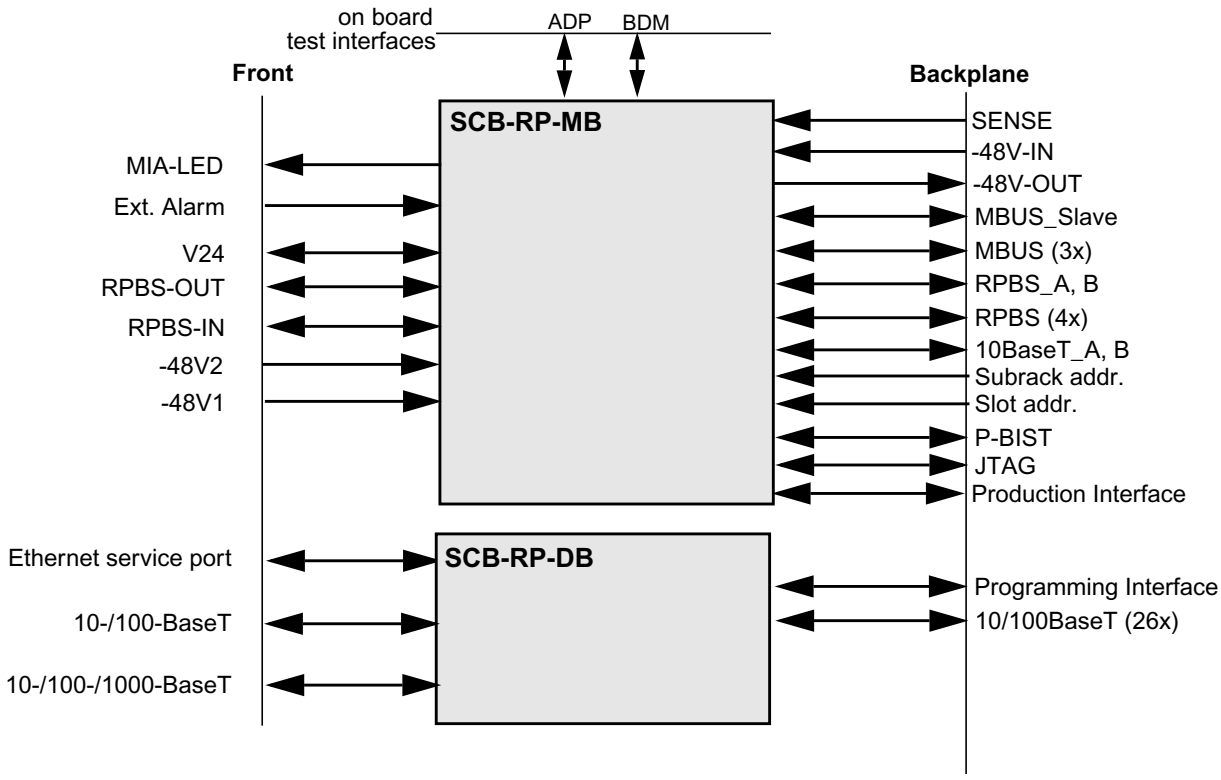


Figure 30: SCB-RP external interface overview

6.1.1 Front interfaces of MB

Table 4: -48V Power Front Interface

Signal name	Signal type	Width	In/ Out	Description
-48V_IN1	-48V	1	I	Unfiltered -48V to supply left half of the GEM sub-rack.
-48V_IN2	-48V	1	I	Unfiltered -48V to supply right half of the GEM sub-rack.

Table 5: RPB-S Front Interface

Signal name	Signal type	Width	In/ Out	Description
TX_I_P TX_I_N	LVDS	2	I	Differential RPB-S data sent from CP to RP.
RX_I_P RX_I_N	LVDS	2	O	Differential RPB-S data sent from RP to CP.
TX_O_P TX_O_N	LVDS	2	O	Differential RPB-S data received from CP and sent to next GEM subrack.
RX_O_P RX_O_N	LVDS	2	I	Differential RPB-S data received from other GEM subrack to be sent to CP.

Table 6: V24 Front Interface

Signal name	Signal type	Width	In/ Out	Description
TXDV24	RS232	1	O	Serial data transmit direction. (SCC1)
RXDV24	RS232	1	I	Serial data receive direction. (SCC1)

Table 7: External Alarm Front Interface

Signal name	Signal type	Width	In/ Out	Description
EXAL_A EXAL_B	bal-anced	2	I	The voltage difference between the two signals, is decisive for generating an alarm.

6.1.2 Front interfaces of DB

Table 8: 1000BaseT - Gigabit Ethernet

Signal name	Signal type	Width	In/ Out	Description
MXP0 MXN0	1000-BaseT	2	I/O	Transmit Receive Pairs. In 1000Base-T mode, differential data from the media is transmitted and received on all four MX+/- signal pairs. In autonegotion, 10Base-T and 100Base-TX modes, MX_0 is transmit and MX_1 is receive pair. Auto-MDIX can reverse the pairs.
MXP1 MXN1	1000-BaseT	2	I/O	
MXP2 MXN2	1000-BaseT	2	I/O	
MXP3 MXN3	1000-BaseT	2	I/O	

Table 9: 10-,100-BaseT - Systemport

Signal name	Signal type	Width	In/ Out	Description
FE26_TXP FE26_TXN	10-/100-BaseT	2	O	Transmit Differential Pair. These pins transmit the serial bit stream.The differential pair is a 2 level signal in 10BaseT mode or a 3-level signal in 100BaseTX mode. These signals are isolated via a transformer.
FE26_RXP FE26_RXN	10-/100-BaseT	2	I	Receive Differential Pair. These pins receive the serial bit bitstream. The differential pair is a 2 level signal in 10BaseT mode or a 3-level signal in 100BaseTX mode. These signals are isolated via a transformer.

Table 10: 10-,100-BaseT - Serviceport

Signal name	Signal type	Width	In/ Out	Description
FE31_TXP FE31_TXN	10-/100-BaseT	2	O	Transmit Differential Pair. These pins transmit the serial bit stream.The differential pair is a 2 level signal in 10BaseT mode or a 3-level signal in 100BaseTX mode. These signals are isolated via a transformer.
FE31_RXP FE31_RXN	10-/100-BaseT	2	I	Receive Differential Pair. These pins receive the serial bit bitstream. The differential pair is a 2 level signal in 10BaseT mode or a 3-level signal in 100BaseTX mode. These signals are isolated via a transformer.

6.1.3 Backplane Interfaces of MB

Table 11: -48V Power Supply

Signal name	Signal type	Width	In/ Out	Description
-48V_OUT1	-48V	2 (connectors)	O	Filtered -48V supply for the left half of GEM subrack.
-48V_OUT2	-48V	2 (connectors)	O	Filtered -48V supply for the right half of GEM subrack.
-48V_A	-48V	1	I	Filtered -48V board supply, derived from A-side SCB-RP board.
-48V_B	-48V	1	I	Filtered -48V board supply, derived from B-side SCB-RP board.

Table 12: Addresses

Signal name	Signal type	Width	In/ Out	Description
BADR[0-4]	GND or open	5	I	Board address, hardcoded in the backplane. The board address is connected to some of the MPC860's GPIOs. It is used for calculating the RP address.
BADRP	GND or open	1	I	Odd parity calculated from the BADR0-BADR4. The board address parity is connected to one of the MPC860's GPIOs.
SR0ADR[0-3]	GND or open	4	I	Subrack address taken from AP-0 used for RP address calculation. The subrack address is connected to the FIA ASIC.
SR0ADRP	GND or open	1	I	Even Parity calculated from SR0ADR0 - SR0ADR3. The subrack address parity is connected to the FIA ASIC.
SR1ADR[0-3]	GND or open	4	I	Subrack address taken from AP-1 is not used on SCB, but is connected to the FIA ASIC.
SR1ADRP	GND or open	1	I	Even Parity calculated from SR1ADR0 - SR1ADR3. The board address parity is connected to the FIA ASIC.
SR2ADR[0-3]	GND or open	4	I	Subrack address taken from AP-2 is not used on SCB, but is connected to the FIA ASIC.
SR2ADRP	GND or open	1	I	Even Parity calculated from SR2ADR0 - SR2ADR3. The board address parity is connected to the FIA ASIC.

Table 13: MBUS master and slave interface

Signal name	Signal type	Width	In/ Out	Description
MBADR[0-4]	GND or open	5	I	Address pins for the MBUS. This same information as board address but is electricaly seperated in the backplane.
MBSDA	LVCMOS	1	I/O	Serial data for the MBUS slave.
MBSCL	LVCMOS	1	I	Serial clock for MBUS slave.
MBWCZ	LVCMOS	1	I	Write Control signal for the MBUS slave. To be used by the production only to program the HWID!
SLAVE_3V	3.3V	1	I	3.3V Power Supply for the MBUS slave on SCB-RP.
SCL_x; x=1-3	LVCMOS	3	O	Serial Clock towards MBUS slaves in GEM.
SDA_x; x=1-3	LVCMOS	3	I/O	Serial Data towards MBUS slaves in GEM.
MB3_3V	3.3V	2 (pins)	O	3.3V power supply for MBUS slaves in GEM.

Table 14: RPB-S backplane interface

Signal name	Signal type	Width	In/ Out	Description
RPBS_RX[1-4]	LVCMOS	4	I	RPBS data from RPIs in GEM towards the CP.
RPBS_TX[1-4]	LVCMOS	4	O	RPBS data from CP towards the RPIs in GEM.
CRD_A	LVCMOS	1	I	RPBS receive data from CP to RP on path A
RCD_A	LVCMOS	1	O	RPBS receive data from RP to CP on path A
CRD_B	LVCMOS	1	I	RPBS receive data from CP to RP on path B
RCD_B	LVCMOS	1	O	RPBS receive data from RP to CP on path B

Table 15: RPI Ethernet Backplane Interface

Signal name	Signal type	Width	In/ Out	Description
RXP_x, RXN_x x=A, B	10BaseT	2 x 2	O	Transmit Differential Pair output from RPI to Ethernet-switch in A and B-side of GEM. These pins transmit the serial bit stream.The differential pair is a 2 level signal in 10BaseT mode. These signals are isolated via a transformer.

Table 15: RPI Ethernet Backplane Interface

Signal name	Signal type	Width	In/ Out	Description
TXP_x, TXN_x x=A, B	10BaseT	2 x 2	I	Receive Differential Pair input to RPI from Ethernet switch located in A-side of GEM. These pins receive the serial bit bitstream. The differential pair is a 2 level signal in 10BaseT mode. These signals are isolated via a transformer.

JTAG

The JTAG interface is used during the manufacturing to load the boot program into the flash memory. This interface will also be used to perform boundary scan tests on the PBA. The signals of the JTAG interface are connected to the backplane.

Table 16: JTAG

Signal name	Signal type	Width	In/ Out	Description
BP_TMS	LVCMOS	1	I	Test Mode Select
BP_TDI	LVCMOS	1	I	Test Data In.
BP_TDO	LVCMOS	1	O	Test Data Out of the FIA.
BP_TRSTZ	LVCMOS	1	I	Test ReSeT (low active) *.
BP_CLK	LVCMOS	1	I	Test Clock.
BP_BYPZ	LVCMOS	1	I	Test BYPass.

***)** It is recommended by Motorola to combine TRSTZ signal of the processor with the power on reset signal or to ground TRSTZ during normal operation.

PBIST

P-Bist interface gives the possibility to do built in self tests of processor and the memory system.

The P-BIST interface on SCB-RP is designed to meet the requirements for P-BIST (see reference /7/).

Table 17: PBIST

Signal name	Signal type	Width	In/ Out	Description
TMPZ	LVCMOS	1	I	Test Mode Pin , will be read at the very beginning of P-BOOT to determine if P-BIST application shall be executed.

Table 17: PBIST

Signal name	Signal type	Width	In/ Out	Description
TRG	LVCMOS	1	O	Trigger. This signal is controlled by P-BIST SW and allows fault tracing for external equipment.
TXD1	RS232	1	O	RS-232 interface used for communication between MPC860 (SCC4) and the external test equipment.
RXD1	RS232	1	I	
PORESETZ	LVCMOS	1	I	Power On Reset.
GND	-	-	O	GND.

Table 18: Other Production Interfaces

Signal name	Signal type	Width	In/ Out	Description
Interface for in-system-programming				
PB31_S0	LVCMOS	1	I	If this signal is low, it is possible to connect to PBOOT via V.24 (RXD1, TXD1). Production will use it to program the OS to the Flashes.
JFWEZ	LVCMOS	1	I	JTAG Flash Write Enable low active.
JENZ	LVCMOS	1	I	JTAG ENable signal for Flash programming low active.
FLWP	LVCMOS	1	I	FLash Write Protect signal. Only to be used by the production.

6.1.4 Backplane Interfaces of DB

Table 19: EEPROM Backplane Interface

Signal name	Signal type	Width	In/ Out	Description
EP_DI	LVCMOS	1	I	Data In signal for programming EEPROM
EP_DO	LVCMOS	1	O	Data Out signal for programming EEPROM
MB_PORSTZ	LVCMOS	1	I/O	Power On Reset for MB, low active
EP_CS	LVCMOS	1	I	Chip Select signal for EEPROM
EP_CLK	LVCMOS	1	I	Clock signal for EEPROM
TRI_360Z	LVCMOS	1	I	Tristate enable signal to be able to perform ISP of the Ethernet EEPROMs, low activ.
TRI_303Z	LVCMOS	1	I	Tristate enable signal to be able to perform ISP of the Ethernet EEPROMs, low activ.

Signal name	Signal type	Width	In/ Out	Description
EP360_DI	LVCMOS	1	I	Data In signal for programming EEPROM, not used
EP360_DO	LVCMOS	1	O	Data Out signal for programming EEPROM, not used
EP360_CS	LVCMOS	1	I	Chip Select signal for EEPROM, not used
EP360_CLK	LVCMOS	1	I	Clock signal for EEPROM, not used
GND	-	-	-	Ground

Table 20: Ethernet Backplane Interface

Signal name	Signal type	Width	In/ Out	Description
FETXP_x, FETXN_x x=0..25	10-/100-BaseT	2 x 26	O	Transmit Differential Pair. These pins transmit the serial bit stream.The differential pair is a 2 level signal in 10BaseT mode or a 3-level signal in 100BaseTX mode. These signals are isolated via a transformer.
FERXP_x, FERXN_x x=0..25	10-/100-BaseT	2 x 26	I	Receive Differential Pair. These pins receive the serial bit bitstream. The differential pair is a 2 level signal in 10BaseT mode or a 3-level signal in 100BaseTX mode. These signals are isolated via a transformer.

6.1.5 External Test Interfaces on Board

This chapter describes additional test interfaces which are not available in the front nor in the backplane connectors. The connector are located on the board, but will not be equipped on the released product.

ADP (MB)

The Advanced Debug Port (ADP) interface is used for debugging during both design verification and software development. The Advanced Debug Port is used to connect the RP control box (see reference /15/) to the RPI. Via this box it is possible to send commands to the OS monitor, download SW to the RPI and connect host debuggers to the debug monitor on the RPI.

Note: This connector will not be mounted on the released products.

Table 21: Signals of ADP interface

RPI signal name	Port name	MPC860 pin	In/ Out	Description
PA8_LED3	PA_8	L17	O	These three signals driving LEDs at the RP control box, indicating the status of PBOOT execution.
PA9_LED2	PA_9	K18	O	
PA10_LED1	PA_10	J17	O	

Table 21: Signals of ADP interface

RPI signal name	Port name	MPC860 pin	In/ Out	Description
PB20_RXD2	PB_20	L16	I	RXD V.24 2 (SMC2)
P21_TXD2	PB_21	K16	O	TXD V.24 2 (SMC2)
PB29_S2	PB_29	E16	I	These three bits are controlled by the RP control box and indicate the start option to choose by PBOOT.
PB30_S1	PB_30	C19	I	
PB31_S0	PB_31	C17	I	
PD8_TXD1	PD_8	W17	O	TXD V.24 2 (SCC4)
PD9_RXD1	PD_9	V17	I	RXD V.24 2 (SCC4)
ADP_HRSTZ	-		I	Generates a hard reset
ADP_SRSTZ	SRESET	V14	I	Generates a soft reset

BDM (MB)

The Background Debug Mode (BDM) interface is used for debugging during both design verification and for software development. It provides a full duplex serial interface between the MPC860's core and an external development tool (Emulator).

The pins on the standard debug port connector are the maximal group needed to support debug port controllers for the MPC860.
Signals described in table 22 will be available in BDM connector.

This connector will not be mounted on the released products.

Table 22: Signals of BDM interface

Signal name		Width (bits)	In/ Out	Description
VFLS[0-1]		1	O	Visible history FLushes Status, indicates the number of instructions that are flushed from the history buffer on this clock.
DSDO		1	O	Development Serial Data Out
DSDI		1	I	Development Serial Data In
DSCK		1	I	Development Serial Clock
HRESETZ		1	I/O	Hard Reset
BDM_SRSTZ		1	I/O	Soft Reset
+3,3V		1	O	Supply voltage 3,3 Volts
GND		1	I/O	Ground

EPSI (DB)

The Ethernet Port Status Interface is used to monitor the status of all ethernet ports. The interface indicates link activity, link speed and collision.

6.2 Internal Interfaces

6.2.1 MB-DB-Interface

6.2.1.1 Ethernet Management Interface

The Ethernet Management Interface allows communication between the MPC860 and the Ethernet switch devices. It connects the GLINK-to-CPU bridge (GT-48330) with the FIA ASIC. It is a subset of FIA's ADB bus. The Ethernet Managment Interface is compromised of 16bit data, 12 bit address and 7 bit controll and clock signals.

6.2.1.2 JTAG

The JTAG interface is the physical extension of the JTAG chain on the MB. It is comprised of 5 signals defined in the standard and an indication towards the MB that this can sense the presence of the DB.

6.2.1.3 I2C

The I2C interface connects the CPU and the temperature supervison circuit on the DB.It allows the CPU to monitor the temperature measured on the DB. The I2C interface is comprised of a clock and a data signal.

6.2.1.4 Miscellaneous Interfaces

Miscellaneous interfaces are:

Table 23: Miscellaneous Interfaces

Signal name	Signal type	Width	Direction	Description
PORESTZ	LVCMOS	1	bidirectional	Power on reset signal. Low activ. Resets MB and DB.
APPL_RSTZ6	LVCMOS	1	MB to DB	Application Reset. Low activ. This signal is controlled by FIA. This signal is not used.
EXT_IRQ6	LVCMOS	1	DB to MB	This interruped line indicates a overtemperature toward FIA. (In the current design a power on reset for MB and DB is generated when the overtemperature limit is reached. So, FIA will not be able to recognize this interrupt.)

6.2.1.5 Power Supply Interface

The DB is supplied with 3.3V from the MB. All other supply voltages needed on the DB (2.5V, 1.8V) are generated out from this 3.3V.

6.2.2 MII

The MII interface is a point-to-point bus used between Ethernet Phys and Ethernet switch devices. It is capable of supporting 10Mb/s and 100Mb/s data rates. It is fully defined in IEEE 802.3 (clause22). The RMII is comprised of a transmit data interface, a receive data interface, 2 status signals and a management interface.

6.2.3 RMII

The RMII interface is a point-to-point bus used between Ethernet Phys and Ethernet switch devices. It is capable of supporting 10Mb/s and 100Mb/s data rates. It is fully defined by the RMII consortium.

The RMII is extended from the MII to use 2-bit data interfaces and to operate at the doubled frequency (50 MHz). The MII is comprised of a transmit data interface, a receive data interface, 2 status signals and a management interface.

The management interface is the same in both MII and RMII.

6.2.4 GMII

The GMII interface is a point-to-point bus used between Gigabit Ethernet Phys and Gigabit Ethernet switch devices. It is capable of supporting 1000Mb/s data rates. It is fully defined in IEEE 802.3 (clause 35).

The GMII is extended from the MII to use 8-bit data interfaces and to operate at higher frequency (125MHz). The GMII is comprised of a transmit data interface, a receive data interface, 2 status signals and a management interface. Most of the signals are physically shared with the MII interface.

The management interface is the same in both MII and GMII.

6.2.5 G-LINK

The G.Link interface is a point-to-point bus comprised of a clock, command-bit, and 16-bit data for each direction (Tx and Rx). The G.Link bus is used to connect a GalNet switch device (like GT-48350 and GT-48360) to a GT-48303A crossbar.

6.3 Usage of GPIOs of the MPC860.

The MPC860's communication processor module (CPM) supports four general-purpose I/O ports - A,B,C, and D. Each signal in the I/O ports can be configured as a general-purpose I/O signal or as a signal dedicated to supporting communications devices, such as SCCs or SMCs. Table 24 shows how the GPIOs of the MPC860 will be used on SCB-RP board.

There is a number of spare GPIOs, which are either marked with 'reserved for RPI' or 'for application'. No pull up resistors are provided on those pins. Therefore it has to be ensured by the OS or the application software that those unused GPIOs are configured as outputs.

Table 24: Usage of MPC860's GPIOs

Port name	MPC860 pin	MPC860 name	SCB-RP signal name	I/O	Description
Port A					
PA_0	U19	CLK8/TOUT4/L1 TCLKB	PA0	O	reserved for future use RPI

Table 24: Usage of MPC860's GPIOs

Port name	MPC860 pin	MPC860 name	SCB-RP signal name	I/O	Description
PA_1	T19	CLK7/TIN4/BRGO4	PA1_E1TCLK	I	TCLK Ethernet 1
PA_2	R18	CLK6/TOUT3/L1RCLKB/BRGCLK2	PA2_E1RCLK	I	RCLK Ethernet 1
PA_3	P17	CLK5/TIN3/BRGOUT3	PA3	O	reserved for future use RPI
PA_4	P19	TOUT2/CLK4	PA4_E2TCLK	I	TCLK Ethernet 2
PA_5	N18	CLK3/TIN2/L1TCLKA/BRGOUT2	PA5_E2RCLK	I	RCLK Ethernet 2
PA_6	M17	BRGCLK1/TOUT1/CLK2	TMPZ	I	P-Bist Test Mode Pin
PA_7	M19	CLK1/TIN1/L1RCLKA/BRGO1	TRG	O	P-Bist TRiGger
PA_8	L17	L1RXDA	PA8_LED3	O	LED3 on ADP
PA_9	K18	L1TXDA	PA9_LED2	O	LED2 on ADP
PA_10	J17	L1RXDB	PA10_LED1	O	LED1 on ADP
PA_11	G16	L1TXDB	PA11	O	reserved for application
PA_12	F17	TXD2	PA12_E2TXD	O	TXD Ethernet 2 (SCC2)
PA_13	E17	RXD2	PA13_E2RXD	I	RXD Ethernet 2 (SCC2)
PA_14	D17	TXD1	PA14	O	V.24 TXD (SCC1)
PA_15	C18	RXD1	PA15	I	V24_RXD (SCC1)
Port B					
PB_14	U18	RSTRT1	PB14	O	EN_MB1Z; enable for MBus branch 1
PB_15	R17	BRGO3	PB15	O	EN_MB2Z; enable for MBus branch 1
PB_16	N16	L1RQA/L1ST4	PB16	O	EN_MB3Z; enable for MBus branch 1
PB_17	P18	L1RQB/L1ST3	PB17_E1TXE	O	TXEN Ethernet 1
PB_18	N17	L1ST2/RTS2	PB18_E2TXE	O	TXEN Ethernet 2
PB_19	N19	L1ST1/RTS1	DB_LUGGEDZ	I	senses the insertion of the DB.
PB_20	L16	SMRXD2/L1CLKOA	PB20_RXD2	I	RXD V.24 2 (SMC2)
PB_21	K16	SMTXD2/L1CLKOB	P21_TXD2	O	TXD V.24 2 (SMC2)

Table 24: Usage of MPC860's GPIOs

Port name	MPC860 pin	MPC860 name	SCB-RP signal name	I/O	Description
PB_22	L19	SMSYN2/SDACK 2	PB22	O	reserved for future use RPI
PB_23	K17	SMSYN1/SDACK 1	PB23	O	reserved for future use RPI
PB_24	J18	SMRXD1	PB24	O	reserved for application (SMC1)
PB_25	J16	SMTXD1	PB25	O	reserved for application (SMC1)
PB_26	F19	I2CSCL/BRGO2	PB26_SCL	O	Serial Clock for I2C, used for temperature supervision and MBUS
PB_27	E19	I2CSDA/BRGO1	PB27_SDA	IO	Serial Data for I2C, used for temperature supervision and MBUS
PB_28	D19	SPIM-ISO/BRGO4	PB28	O	reserved for application
PB_29	E16	SPIMOSI	PB29_S2	I	Start mode bits 0..2; used to define different start option for PBOOT and OS
PB_30	C19	SPICLK/RSTRT2	PB30_S1	I	
PB_31	C17	REJECT1/SPI-SEL	PB31_S0	I	
Port C					
PC_4	T17	CD4/L1RSYNCA	PC4_BADR0	I	board address bit 0
PC_5	T18	CTS4/L1TSYNC A/SDACK1	PC5_BADR1	I	board address bit 1
PC_6	R19	L1RSYNCB/CD3	PC6_E1RXE	I	RX enable Ethernet 1
PC_7	M16	CTS3/L1TSYNC B/SDACK2	PC7_E1CD	I	Collision detect Ethernet 1
PC_8	M18	PC[8]/CD2/TGAT E2	PC8_E2RXE	I	RX enable Ethernet 2
PC_9	L18	CTS2	PC9_E2CD	I	Collision detect Ethernet 2
PC_10	K19	CD1/TGATE1	PC10_BADR2	I	board address bit 2
PC_11	J19	CTS1	PC11_BADR3	I	board address bit 3
PC_12	F18	L1RQA/L1ST4	PC12_BADR4	I	board address bit 4
PC_13	E18	L1RQB/L1ST3	PC13	I	PFAILA1; -48V power supervision
PC_14	D18	DREQ1/RTS2/L1 ST2	PC14	I	PFAILB1; -48V power supervision
PC_15	D16	DREQ0/RTS1/L1 ST1	PC15	O	reserved for application
Port C					

Table 24: Usage of MPC860's GPIOs

Port name	MPC860 pin	MPC860 name	SCB-RP signal name	I/O	Description
PD_3	W16	REJECT4	PD3_ADRP	O	parity for board address bits 0 - 4
PD_4	U16	REJECT3	PD4	I	PFAILA2; -48V power supervision
PD_5	U15	REJECT2	PD5	I	PFAILB2; -48V power supervision
PD_6	V16	RTS4	PD6	O	reserved for application
PD_7	T15	RTS3	PD7	O	reserved for application
PD_8	W17	TXD4	PD8_TXD1	O	TXD V.24 2 (SCC4)
PD_9	V17	RXD4	PD9_RXD1	I	RXD V.24 2 (SCC4)
PD_10	W18	TXD3	PD10_E1TXD	O	TXD Ethernet 1 (SCC3)
PD_11	T16	RXD3	PD11_E1RXD	I	RXD Ethernet 1 (SCC3)
PD_12	R16	L1RSYNCB	PD12	O	reserved for application
PD_13	V18	L1TSYNCB	PD13	O	reserved for future use RPI
PD_14	V19	L1RSYNCA	PD14	O	reserved for future use RPI
PD_15	U17	L1TSYNCA	PD15	O	reserved for application

6.4 Ethernet Port Mapping

The following table shows how the external Ethernet ports are assigned to the specific integrated circuits and the GLink.

Table 25: Ethernet Port Mapping

Port	Switch Device	Switch Device Port	PHY Device	Phy Device Port	G-LINK Number
Backplane Ports					
0	D13	1	D16	1	4
1	D13	0	D16	0	4
2	D9	6	D12	6	3
3	D9	7	D12	7	3
4	D9	4	D12	4	3
5	D9	5	D12	5	3
6	D9	2	D12	2	3
7	D9	3	D12	3	3

Table 25: Ethernet Port Mapping

Port	Switch Device	Switch Device Port	PHY Device	Phy Device Port	G-LINK Number
8	D9	0	D12	0	3
9	D9	1	D12	1	3
10	D5	6	D8	6	2
11	D5	7	D8	7	2
12	D5	4	D8	4	2
13	D5	5	D8	5	2
14	D5	2	D8	2	2
15	D5	3	D8	3	2
16	D5	0	D8	0	2
17	D5	1	D8	1	2
18	D1	6	D4	6	1
19	D1	7	D4	7	1
20	D1	4	D4	4	1
21	D1	5	D4	5	1
22	D1	2	D4	2	1
23	D1	3	D4	3	1
24	D1	0	D4	0	1
25	D1	1	D4	1	1
Front Ports					
G-Bit	D24	0	D22	0	0
10-/100-BaseT	D13	6	D16	6	4
Service Port	D13	7	D16	7	4
Unused Ports					
	D13	2	D16	2	4
	D13	3	D16	3	4
	D13	4	D16	4	4
	D13	5	D16	5	4

6.5 Power Supply

The SCB-RP board requires three different voltage to be supplied, +3,3V, +1.8V and 2.5V.

The +3.3V is needed for all logic and IOs on MB and DB board.

On MB the +1.8V is only needed for the core supply of the FIA ASIC. No other logic requires this +1.8V supply. The current needed is about 200 mA.

The +2.5V is needed on DB only. It is used for the core supply of the Ethernet switch components (GT-48303A, GT-48350, GT-48360, BCM5401). The current needed is about 3500 mA.

On DB the 1.8V is needed for the core supply of the BCM5401. No other logic requires this 1.8V supply. The current needed is about 300 mA (max).

The total power consumption of the SCB-RP PIU is estimated to 25-30 Watts. These values are based on the estimated values described in table 26 and table 27.

Table 26: Power consumption MB

Part	Max. estimated power consumption	Typ. estimated power consumption
MPC860P	900 mW	600 mW
FIA	900 mW	500 mW
SDRAM (4 devices)	1200 mW	900 mW
Clock distribution (RPI)	340 mW	300 mW
Ethernet Phys	660 mW	550 mW
MBUS slaves (14 slaves)	700 mW	150 mW
Sum for 3.3V, 1.8V	**4700**	**3000 mW**

Table 27: Power consumption DB

Part	Max. estimated power consumption	Typ. estimated power consumption
GT-48303A	1600 mW	
GT48330	500 mW	
GT-48350 (4x)	7000 mW	
LXT9784	10.000 mW	
GT-48360	1250 mW	
BCM5401	4000 mW	
Clock distribution	900 mW	
Sum for 3.3V, 2.5V, 1.8V	**25.150 mW**	

7 Components

The main components used on SCB-RP are listed in table 28.

Table 28: Main components

PBA	Component	Type /Vendor	Product number	Package]	Qty
MB	CPU	MPC860P/ Motorola	RYT 123 6085/1	PBGA 357	1
	FIA	ASIC/ TI	ROP 101 12	BGA 432	1
	SDRAM	KM416S4030AT/ Samsung	RYT 119 106/C	TSOP 54 (II)	4
	Flash	RC28F320C3/ Intel	RYT 118 6152/4	EBGA64	2
	10Base-T Phy	LXT905	RYT 121 159/2C	LQFP32	2
	DC/DC con-verter	PKM4501 Ericsson	RYT9136009/2		1
DB	Ethernet 8-port switch 10/100 MBit	GT-48350/ Galileo Technology	RYT 121 6188/1	PQFP160	4
	Ethernet switch 10/100/1000 MBit	GT-48360 Galileo Technology	RYT 121 6189/1	LQFP128	1
	Crossbar Switch	GT-48303A/ Galileo Technology	RYT 121 6186/1	PBGA456	1
	CPU Bridge	GT-48330/ Galileo Technology	RYT 121 6187/1	PQFP100	1
	10/100 Mbit Octal Phy	LXT9784/ Level1	RYT 121 6172/1	PBGA324	4
	10/100/1000Mbit Single Phy	BCM5401/ Broadcom	RYT 121 6191/1	TBGA256	1

Table 29 shows the programmable components on SCB-RP. All of them are in-system-programmable.

Table 29: Programmable components

Component	Type /Vendor	Product number	Package]	Qty
Switch--EPROM	93C86	RYT 118 6080/1	SO8	1
Flash	RC28F320C3/ Intel	RYT 118 6152/4		2

8 Mechanical Design

8.1 PCB

Table 30: PCB Characteristics of MB

Board	TVJ 828 323/1	Comments
Size [mm]	265mm x 207,5mm (TVJ828)	Required
Thickness [mm]	2,0 +/- 0,2 mm	
Number of Layers	10	
Number of Signal -Layers	6	
Technology	Layer Spec 1301-BYC 101 347 Uen Layer Drawing UAB105 83-010 Uen	
Impedance	single ended: 70 Ohm balanced: 100 Ohm	
Width [mil]	5 and 6 mil	
Conductor [pattern class]	55	
Conductor spacing [pattern class]	55	
Land pattern class	55	
Remarks	None	
Risks	None	

Table 31: PCB Characteristics of DB

Board	TVJ 828 01/1	Comments
Size [mm]	265mm x 207,5mm (TVJ828)	Required
Thickness [mm]	2,05 +/- 0,2 mm	
Number of Layers	14	
Number of Signal -Layers	8 (only 6 are used)	
Technology	see reference /9/	
Impedance	single ended: 54Ohm balanced: 100 Ohm	

Table 31: PCB Characteristics of DB

Board	TVJ 828 01/1	Comments
Width [mil]	4 and 5mil	
Conductor [pattern class]	55	
Conductor spacing [pattern class]	55	
Land pattern class	55	
Remarks	None	
Risks	None	

8.2 PBA - PIU

The PBA shall use the building practice known as the Module Packing System BYB 501+.

Surface mounted and hole mounted components are used. Components are assembled on the primary and secondary side.
The SCB-RP has ESD areas on MB and DB.
Stiffener are not used.
Mechanical guidance and slotcoding is used.

The spacing in subrack needed for the SCB-RP PIU is 30mm.

Soldering process: Reflow soldering on primary and secondary side.

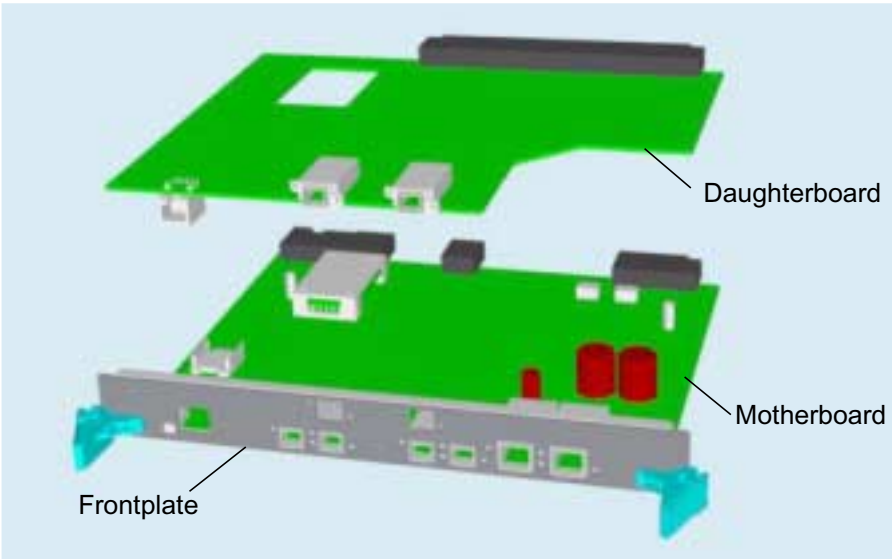
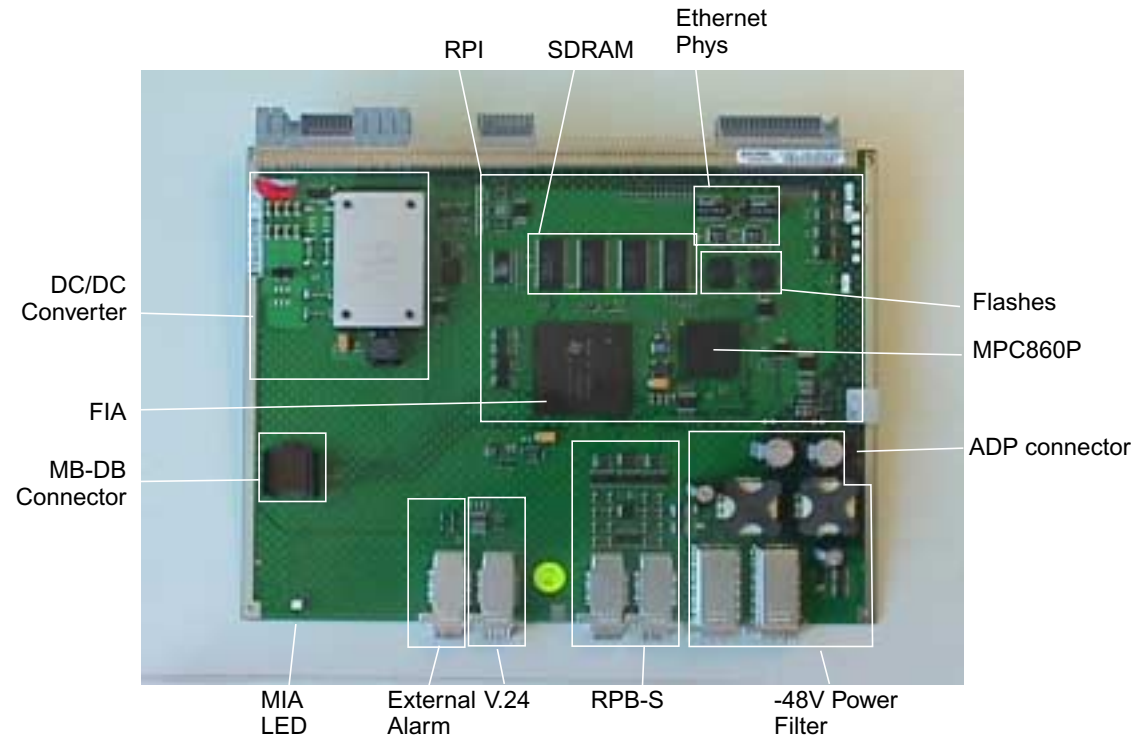


Figure 31: 3D-View of SCB-RP PIU

8.3 Images of hardware



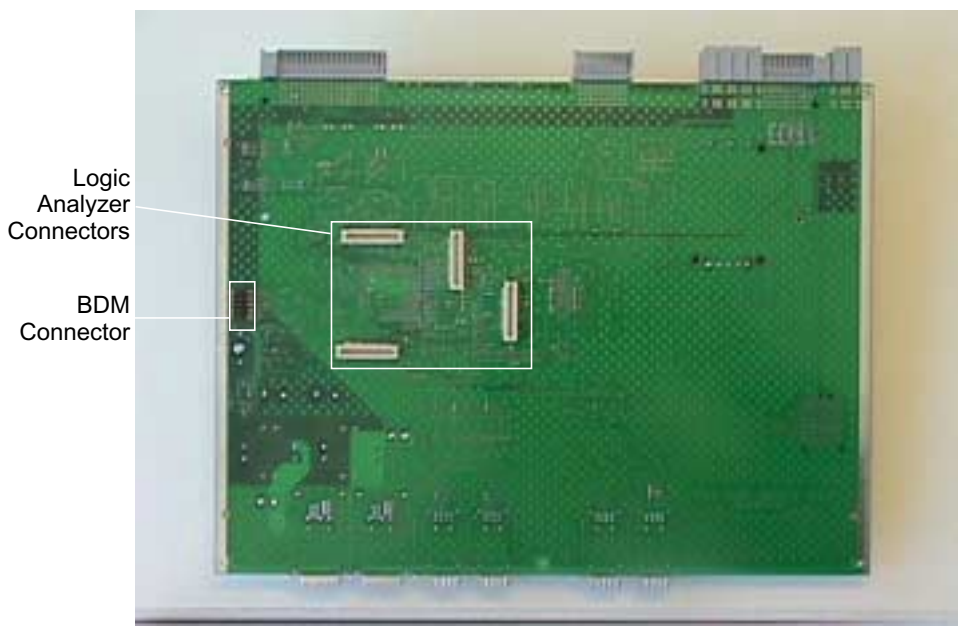


Figure 32: View of SCB-RP-MB primary and secondary side

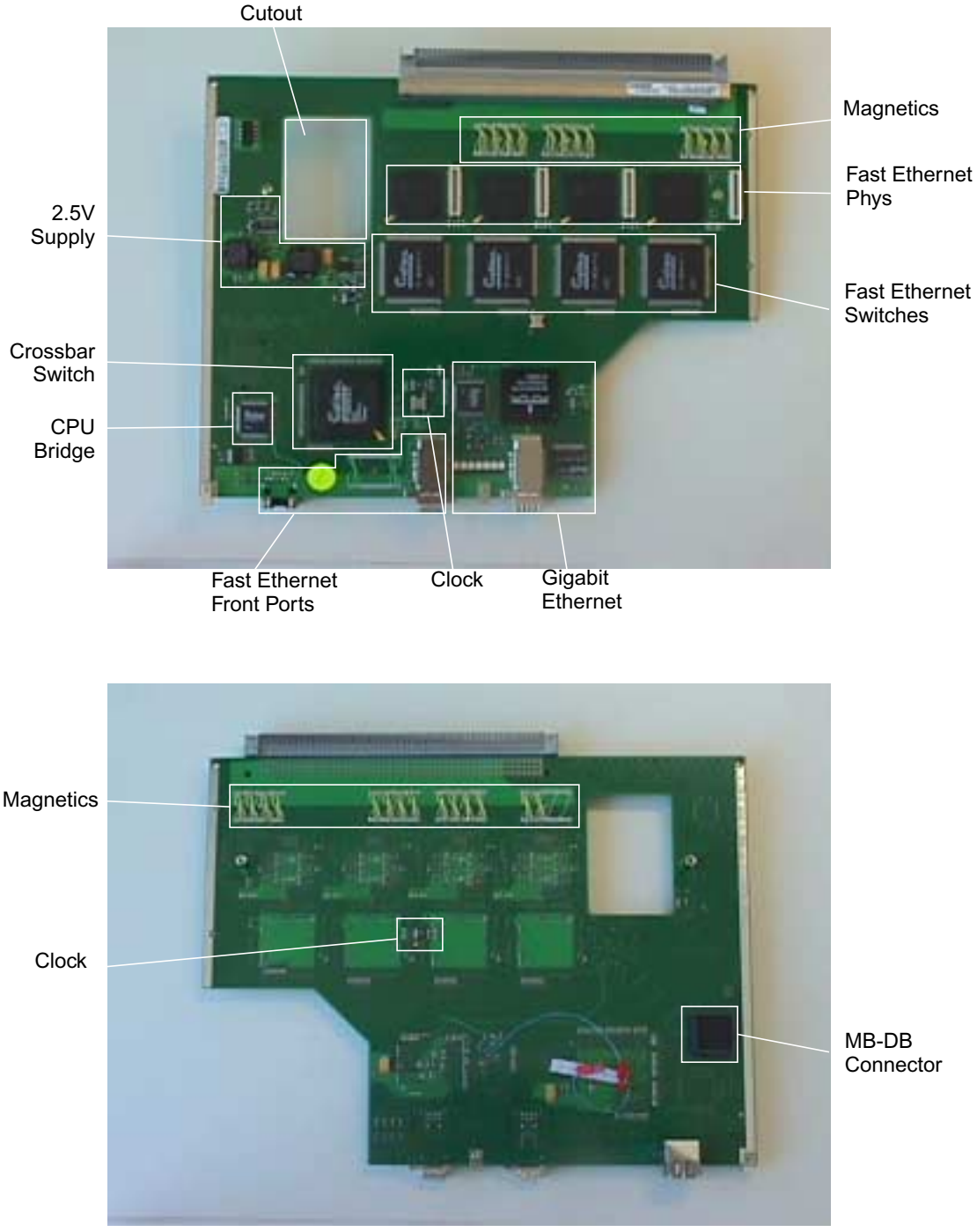


Figure 33: View of SCB-RP-DB primary and secondary side

8.4 Connector Pin Allocation

8.4.1 Front Connectors

8.4.1.1 Front Connector Allocation

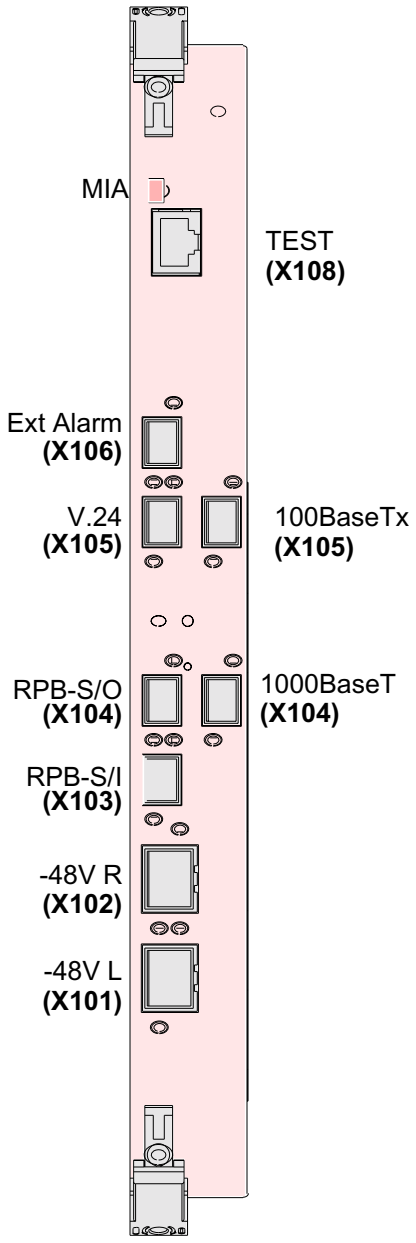


Figure 34: Front plate

8.4.1.2 Front Connectors Motherboard

Table 32: X101 -48V1

ROW	COLUMN	
	A1	A2
A	-48V_IN1	GND
B	-48V_IN1	GND
C	-48V_IN1	GND
D	-48V_IN1	GND
E	-48V_IN1	GND
F	-48V_IN1	GND

Table 33: X102 -48V2

ROW	COLUMN	
	A1	A2
A	-48V_IN2	GND
B	-48V_IN2	GND
C	-48V_IN2	GND
D	-48V_IN2	GND
E	-48V_IN2	GND
F	-48V_IN2	GND

Table 34: X103 RPBS-IN

ROW	COLUMN	
	A	B
1	TX_I_P	RX_I_N
2	RX_I_P	TX_I_N
3	B4 *	A4 *
4	B3 *	A3 *

Table 35: X104 RPBS-OUT

ROW	COLUMN	
	A	B
1	TX_O_P	RX_O_N
2	RX_O_P	TX_O_N
3	B4 *	A4 *
4	B3 *	A3 *

Green shadowed pins are cross connected with the mentioned pin via a 100Ohms resistor.

Table 36: X105 V.24

ROW	COLUMN	
	A	B
1	NC	NC
2	NC	TXDV24
3	RXDV24	NC
4	NC	NC

Table 37: X106 External Alarm

ROW	COLUMN	
	A	B
1	NC	NC
2	EXAL_B	NC
3	NC	EXAL_A
4	NC	NC

8.4.1.3 Front Connectors Daughter Board

Table 38: X104 Gigabit Ethernet Port - RPV 431 1911

ROW	COLUMN	
	A	B
1	MXN3	MXN0
2	MXP0	MXP3
3	MXP1	MXN2
4	MXP2	MXN1

:

Table 39: X105 Ethernet System Port - RPV 431 1911

ROW	COLUMN	
	A	B
1	TERM	FE26_TXN
2	FE26_TXP	TERM
3	FE26_RXP	TERM
4	TERM	FE26_RXN

Table 40: X108 Ethernet Service Port - RNV89986/08

PIN	Signal
1	FE31_RXP
2	FE31_RXN
3	FE31_TXP
4	TERM
5	TERM
6	FE31_TXN
7	TERM
8	TERM

Green shadowed pins are connected to a resistor network to terminate the unused twisted pairs of the cable.

8.4.2 Backplane Connectors

8.4.2.1 Backplane Connectors on MB

Table 41. X01_MB

ROW	COLUMN				
	A	B	C	D	E
01	SENSE_UP	MBWCZ	GND	BP_TCK	BP_TRSTZ
02	MBADR0	MBADR1	GND	MBADR2	MBADR3
03	MBADR4	MBSDA	GND	BP_TDI	BP_TMS
04	MBSCL	SLAVE_3V	GND	BP_TDO	BP_BYPZ
05	NC	NC	GND	MB3_3V	MB3_3V
06	JTAG-BUS-term0	JTAG-BUS-term1	GND	JTAG-BUS-term2	JTAG-BUS-term3
07	SCL1	NC	GND	SDA1	NC
08	SCL2	NC	GND	SDA2	NC
09	SCL3	NC	GND	SDA3	NC
10	PSVA1	PSVA2	GND	PSVB1	PSVB2

Table 42. X05_MB

ROW	COLUMN				
	A	B	C	D	E
01	NU	NU	GND	NU	NU
02	NU	NU	GND	NU	NU
03	NU	NU	GND	NU	NU
04	NU	NU	GND	NU	NU
05	NU	NU	GND	NU	NU
06	NU	NU	GND	NU	NU
07	NU	NU	GND	NU	NU
08	NU	NU	GND	NU	NU
09	NU	NU	GND	NU	NU
10	NU	NU	GND	NU	NU

Note: All pins of X05 of the MB are connected one-to-one to X05 of DB. Green marked pins are used on DB for test or production purpose.

Table 43. X10_MB

ROW	COLUMN				
	A	B	C	D	E
01	TXP_A	TXN_A	GND	TXN_B	TXP_B
02	RXP_A	RXN_A	GND	RXN_B	RXP_B
03	Future 1000BaseT	Future 1000BaseT	GND	Future 1000BaseT	Future 1000BaseT
04	Future 1000BaseT	Future 1000BaseT	GND	Future 1000BaseT	Future 1000BaseT
05	NC	NC	GND	NC	SR0ADRP
06	SR0ADR0	SR0ADR1	GND	SR0ADR2	SR0ADR3
07	TX_1	TX_2	GND	TX_3	TX_4
08	RX_1	RX_2	GND	RX_3	RX_4
09	NC	CRD_A	GND	CRD_B	NC
10	NC	RCD_A	GND	RCD_B	NC

Table 44. X11_MB

ROW	COLUMN				
	A	B	C	D	E
01	SR1ADR0	SR1ADR1	GND	SR1ADR2	SR1ADR3
02	SR1ADRP	SR3ADR0	GND	SR3ADR1	SR3ADR2

Table 44. X11_MB

ROW	COLUMN				
	A	B	C	D	E
03	SR3ADR3	SR3ADRP	GND	BADR0	BADR1
04	BADR2	BADR3	GND	BADR4	BADRP
05	NC	NC	GND	NC	NC
06	NC	NC	GND	NC	JFWEZ
07	PB_RSTZ	TRG	GND	FLWP	NC
08	P3V	GND	GND	TMPZ	PB31_S0
09	NC	TXD1	GND	RXD1	NC
10	SENSE_DOWN	NC	GND	NC	NC

Connector pins not connected in the backplane are shadowed (green).

Table 45: XP01, XP02 and XP03

Connector	Pin	
	1-4	5-8
XP01	GND	-48V_A
XP02	GND	-48V_B
XP03	GND	-48V_OUT1
XP04	GND	-48V_OUT1
XP05	GND	-48V_OUT2
XP06	GND	-48V_OUT2

8.4.2.2 Backplane Connectors on DB

Table 46. X05_DB

ROW	COLUMN				
	A	B	C	D	E
01	EP_DI	EP_CS	GND	EP360_DI	EP360_CS
02	EP_DO	EP_CLK	GND	EP360_DO	EP360_CLK
03	MB_PORSTZ	TRI_360Z	GND		
04		TRI_303Z	GND		
05			GND		
06			GND		
07			GND		
08			GND		
09			GND		
10			GND		

Note: Connector pins D01-D02 and pins E01-E02 are not used.

Table 47. X06_DB

ROW	COLUMN				
	A	B	C	D	E
01	FETXP0	FETXN0	GND	1000BaseT_TXP_0	1000BaseT_TXN_0
02	FERXP0	FERXN0	GND	1000BaseT_RXP_0	1000BaseT_RXN_0
03	FETXP1	FETXN1	GND	1000BaseT_TXP_1	1000BaseT_TXN_1
04	FERXP1	FERXN1	GND	1000BaseT_RXP_1	1000BaseT_RXN_1
05	FETXP2	FETXN2	GND	1000BaseT_TXP_2	1000BaseT_TXN_2
06	FERXP2	FERXN2	GND	1000BaseT_RXP_2	1000BaseT_RXN_2
07	FETXP3	FETXN3	GND	1000BaseT_TXP_3	1000BaseT_TXN_3
08	FERXP3	FERXN3	GND	1000BaseT_RXP_3	1000BaseT_RXN_3
09	FETXP4	FETXN4	GND	1000BaseT_TXP_4	1000BaseT_TXN_4
10	FERXP4	FERXN4	GND	1000BaseT_RXP_4	1000BaseT_RXN_4

Table 48. X07_DB

ROW	COLUMN				
	A	B	C	D	E
01	FETXP5	FETXN5	GND	1000BaseT_TXP_5	1000BaseT_TXN_5
02	FERXP5	FERXN5	GND	1000BaseT_RXP_5	1000BaseT_RXN_5
03	FETXP6	FETXN6	GND	1000BaseT_TXP_6	1000BaseT_TXN_6
04	FERXP6	FERXN6	GND	1000BaseT_RXP_6	1000BaseT_RXN_6
05	FETXP7	FETXN7	GND	1000BaseT_TXP_7	1000BaseT_TXN_7
06	FERXP7	FERXN7	GND	1000BaseT_RXP_7	1000BaseT_RXN_7
07	FETXP8	FETXN8	GND	1000BaseT_TXP_8	1000BaseT_TXN_8
08	FERXP8	FERXN8	GND	1000BaseT_RXP_8	1000BaseT_RXN_8
09	FETXP9	FETXN9	GND	1000BaseT_TXP_9	1000BaseT_TXN_9
10	FERXP9	FERXN9	GND	1000BaseT_RXP_9	1000BaseT_RXN_9

Table 49. X08_DB

ROW	COLUMN				
	A	B	C	D	E
01	FETXP10	FETXN10	GND	1000BaseT_TXP_10	1000BaseT_TXN_10
02	FERXP10	FERXN10	GND	1000BaseT_RXP_10	1000BaseT_RXN_10
03	FETXP11	FETXN11	GND	1000BaseT_TXP_11	1000BaseT_TXN_11
04	FERXP11	FERXN11	GND	1000BaseT_RXP_11	1000BaseT_RXN_11
05	FETXP12	FETXN12	GND	1000BaseT_TXP_12	1000BaseT_TXN_12
06	FERXP12	FERXN12	GND	1000BaseT_RXP_12	1000BaseT_RXN_12
07	FETXP13	FETXN13	GND	1000BaseT_TXP_13	1000BaseT_TXN_13

Table 49. X08_DB

ROW	COLUMN				
	A	B	C	D	E
08	FERXP13	FERXN13	GND	1000BaseT_RXP_13	1000BaseT_RXN_13
09	FETXP14	FETXN14	GND	1000BaseT_TXP_14	1000BaseT_TXN_14
10	FERXP14	FERXN14	GND	1000BaseT_RXP_14	1000BaseT_RXN_14

Table 50. X09_DB

ROW	COLUMN				
	A	B	C	D	E
01	FETXP15	FETXN15	GND	1000BaseT_TXP_15	1000BaseT_TXN_15
02	FERXP15	FERXN15	GND	1000BaseT_RXP_15	1000BaseT_RXN_15
03	FETXP16	FETXN16	GND	1000BaseT_TXP_16	1000BaseT_TXN_16
04	FERXP16	FERXN16	GND	1000BaseT_RXP_16	1000BaseT_RXN_16
05	FETXP17	FETXN17	GND	1000BaseT_TXP_17	1000BaseT_TXN_17
06	FERXP17	FERXN17	GND	1000BaseT_RXP_17	1000BaseT_RXN_17
07	FETXP18	FETXN18	GND	1000BaseT_TXP_18	1000BaseT_TXN_18
08	FERXP18	FERXN18	GND	1000BaseT_RXP_18	1000BaseT_RXN_18
09	FETXP19	FETXN19	GND	1000BaseT_TXP_19	1000BaseT_TXN_19
10	FERXP19	FERXN19	GND	1000BaseT_RXP_19	1000BaseT_RXN_19

Table 51. X10_DB

ROW	COLUMN				
	A	B	C	D	E
01	FETXP20	FETXN20	GND	1000BaseT_TXP_20	1000BaseT_TXN_20
02	FERXP20	FERXN20	GND	1000BaseT_RXP_20	1000BaseT_RXN_20
03	FETXP21	FETXN21	GND	1000BaseT_TXP_21	1000BaseT_TXN_21
04	FERXP21	FERXN21	GND	1000BaseT_RXP_21	1000BaseT_RXN_21
05	FETXP22	FETXN22	GND	1000BaseT_TXP_22	1000BaseT_TXN_22
06	FERXP22	FERXN22	GND	1000BaseT_RXP_22	1000BaseT_RXN_22
07	FETXP23	FETXN23	GND	1000BaseT_TXP_23	1000BaseT_TXN_23
08	FERXP23	FERXN23	GND	1000BaseT_RXP_23	1000BaseT_RXN_23
09	FETXP24	FETXN24	GND	1000BaseT_TXP_24	1000BaseT_TXN_24
10	FERXP24	FERXN24	GND	1000BaseT_RXP_24	1000BaseT_RXN_24

Table 52. X11_DB

ROW	COLUMN				
	A	B	C	D	E
01	FETXP25	FETXN25	GND	1000BaseT_TXP_25	1000BaseT_TXN_25
02	FERXP25	FERXN25	GND	1000BaseT_RXP_25	1000BaseT_RXN_25
03	NU	NU	GND	NU	NU
04	NU	NU	GND	NU	NU
05	NU	NU	GND	NU	NU
06	NU	NU	GND	NU	NU
07	NU	NU	GND	NU	NU
08	NU	NU	GND	NU	NU
09	NU	NU	GND	NU	NU
10	NU	NU	GND	NU	NU

8.4.3 MB-DB connector

Table 53. MB-DB IF (100 pin) RPV 640 2111/01, RNV 640 2112/01

ROW	COLUMN									
	A	B	C	D	E	F	G	H	I	J
01	EMDAT_0	EMDAT_1	GND	EMDAT_2	EMDAT_3	EMDAT_4	EMDAT_5	GND	EMDAT_6	EMDAT_7
02	EMDAT_8	EMDAT_9	GND	EMDAT_10	EMDAT_11	EMDAT_12	EMDAT_13	GND	EMDAT_14	EMDAT_15
03	EMADD_1	EMADD_2	GND	EMADD_3	EMADD_4	EMADD_5	EMADD_6	GND	EMADD_7	EMADD_8
04	EMADD_9	EMADD_10	GND	EMADD_11	EMTSZ	EMTAZ	EMINTZ	GND	EMRD	EMWRZ
05	EMCS	CLK_EM	GND	DB_TCK	DB_TRSTZ	DB_TDI	DB_TDO	GND	DB_TMS	NC
06	MPC_SDA (I2C)	MPC_CLK (I2C)	GND	PORESETZ	PORESET	HRESETZ	NC	GND	SENSE_DB	NC
07	PB22	PB23	GND	PD6	PD7	IRQ4	IRQ6	GND	CS2	CS3
08	APPL_RSTZ7	APPL_RSTZ6	GND	NC	NC	EXT_IRQ5	EXT_IRQ6	GND	ACS6_CCS1	ACS5_CCS2
09	NC	NC	GND	NC	NC	NC	NC	GND	NC	NC
10	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V
K1 - K72	GND									
K73 - K90	3.3V									

Green shadowed pins are connected on the MB, but not used on DB.

8.4.4 Test connectors

Table 54: BDM connector

Pin	Signal	Pin	Signal
1	VFLS0	2	BDM_SRSTZ
3	GND	4	DSCK
5	GND	6	VFLS1
7	HRESETZ	8	DSDI
9	+3,3V	10	DSDO

Table 55: ADP connector

Pin	Signal	Pin	Signal
1	RXD2	2	PB31_S0
3	TXD2	4	PB30_S1
5	RXD1	6	PB29_S2
7	TXD1	8	nc
9	nc	10	ADP_SRSTZ
11	GND	12	ADP_HRSTZ
13	nc	14	LED1
15	nc	16	LED2
17	nc	18	LED3
19	nc	20	nc

9 Verification and Test

9.1 Boundary Scan Chain on the SCB-RP

The SCB-RP contains 5 components supporting boundary scan according to JTAG standard IEEE 1149.1. The chain connects MB and DB via the MB-DB-Interface. It is automatically detected wether the daughter card is plugged onto the MB. This allows to use the JTAG chain on a standalone MB.
The boundary scan chain on SCB-RP is shown in the following figure.

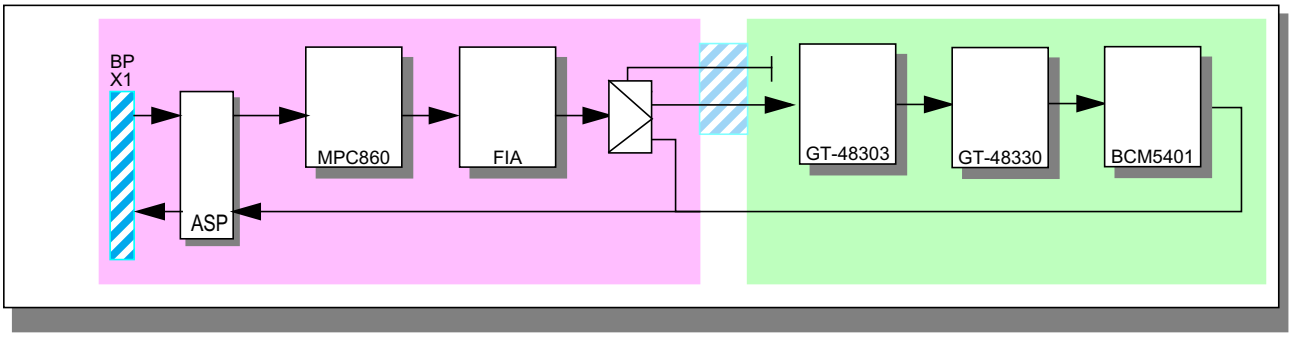


Figure 35: Boundary Scan Chain of the SCB-RP

The simplified figure above shows the signal flow of the test data signal. Of course, the remaining signals TRSTZ, TMS, TCLK are distributed to all devices separately.

9.2 Design for Basic Test

The SCB-RP board includes the following features to support the verification process during Basic Test:

- BDM interface. For debugging and testing of the MPC with help of an emulator.
- ADP interface. For debugging and testing of the MPC with help of the RP Tool Box.
- MPC-bus test connectors. These connectors allow the observation of the processor bus by connecting a logic analyser to the test connectors.
- LED connectors, which allows to monitor port status LEDs of the Ethernet links.

Note: All the mentioned test connectors are not mounted on the final product.

9.3 Design for Production Test

The SCB-RP board provides Boundary Scan functionality for production test.

The SCB-RP board is prepared to support P-BIST via the backplane.

10 Environmental Requirements

10.1 Reliability

The mean time to failure (MTTF) at 25degC ambient temperature is at least 78 years on the SCB-RP board.

10.2 Temperature

According to reference /6/, the SCB-RP board fulfils the following temperature ranges:

Normal operation: + 5degC ... +40degC
Safe operation: - 5degC ... +50degC
Non destruction: -10degC ... +55degC

10.3 EMC

The SCB-RP board complies with requirements stated in reference /5/.

10.4 ESD

The SCB-RP board complies with requirements stated in reference /5/.

11 Abbreviations

Abbreviation	Explanation
ADB	Application Device Bus
ADP	Advanced Debug Port
ASIC	Application Specific Integrated Circuit
AUI	Attachment Unit Interface
BDM	Background Debug Mode interface
BGA	Ball Grid Array
BIST	Built In Self Test
BP	Backplane
BYB 501	An Ericsson standard of equipment practice
CP	Central Processor in AXE-10 terminology.
CPU	Central Processing Unit
DB	DaughterBoard
DL34	Digital Link adaptable from version 3 to 4
DMA	Direct Memory Access
DRAM	Dynamic Random-Access Memory
EMC	ElectroMagnetic Compatibility
EPSI	Ethernet Port Status Interface
ESD	ElectroStatic Discharge
Ethernet	Local Area Network IEEE 802.3
FIA	A MPC860 support ASIC developed at UAB
GEM	Generic Ericsson Magazine
GDM-H	Generic Device Magazine for Half height boards
HWM	HardWare Modernisation program for AXE
I^2C	Inter-IC bus.
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IP	Implementation Proposal or Internet Protocol
ISP	In-System-Programming
JTAG	Joint Test Action Group, IEEE 1149.1
LED	Light Emitting Diode
MB	MotherBoard
MIA	Manual Intervention Allowed
MII	Media Independent Interface (Ethernet)
MIPS	Mega Instructions Per Second
MTC	Master Test Controller

Abbreviation	Explanation
MTTF	Mean Time To Failure
O&M	Operation and Maintenance
PBA	Printed Board Assembly, a PCB with mounted components.
P-BIST	Processor Controlled Built In Self Test
PCB	Printed Circuit Board
PDU	Power Distribution Unit
Phy	Physical Interface circuit (for Ethernet)
PLL	Phase Locked Loop
PPC	PowerPC
PQFP	Plastic Quad Flat Pack
RP	Regional Processor
RPB	Regional Processor Bus
RPB-S	Serial RP Bus
RPG	Regional Processor with Group Switch Interface
RPI	Regional Processor Integrated (hardware module)
SCC	Serial Communication Controller
SDRAM	Synchronous DRAM
SMC	Serial Management Controller
TAP	Test Access Port
UART	Universal Asynchronous Receiver Transmitter
UPM	User Programmable Machine
V.24	ITU-T standard for serial communication. Similar to the IEC standard RS-232.