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REGIONAL PROCESSOR SUBSYSTEM, RPS-2

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1 Revision Information

PD1: Rev C updated due to extensions of RP2 and RPD processors families with Regional Processors connected to the RPB-S.

PD2: Some minor updatings introduced.

PD3: Updated after internal review by subsystem responsible.

2 General

The Regional Processor Subsystem RPS-2 contains the Regional Processor family RP2 with microprogram and executive program and the Regional Processor family RPD with operative systems of the included members.

The subsystem contains software for the maintenance function, restart dump and software for the following support functions: program test and program correction.

2.1 General RP2 family

RP2 is a family of processors which includes a number of processors with standardized interface (EMB) for HW control.

The functions implemented in subsystem RPS-2 are not dependent on CP version used.

The members of the family are:

a RP2

RP2 is a modernized version of the previous RP, RP1, in AXE 10.

b RP4

RP4 has mainly the same functionality as the RP2 but is connected to the RPB-S. Additional functionality in the RP4 have been introduced due to the fact that the processor is also responsible for power distribution in a new BYB 501 magazine (GDM-H or GDM-F).

The hardware controlled by the members of RP2 family is organized in a number of Extension Modules (EMs). Each EM includes a specific number of hardware units (devices or switches). The number of hardware units per EM can vary between different device types.

The EMs are connected to the members of RP2 family by the EM Bus (EMB). Each EM is normally connected to two members (of the same sort) of the RP2 family, forming an RP pair. The second RP in a pair is called the twin RP, see figure 1. Each RP pair controls a set of EMs. The number of EMs connected to an RP pair is varying depending on the capacity demands in RP up to 16.

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Each RP in the pair normally controls half of the connected EMs. If a fault occurs in one RP2/RP4, the other RP2 respectively RP4 in the pair, takes over the control of all connected EMs.

This duplication of RP2/RP4 is optional. If the demands on availability for a certain type of hardware is not so high, then only one member of the RP2 family may be used for controlling that hardware.

All interwork between CP and members of the RP2 family is carried out through the transmission of messages, signals, over the Regional Processor Bus, RPB.

The addressing of signals from CP to the regional software units in RP2/RP4 are defined by the RP-address and the CM (Control Module). The data store for the programs in the RP2/RP4 is always unique for each CM. However the program code can be shared by several CMs.

No interwork takes place between different CMs or between different members of the RP2 family. Normally each CM corresponds to one EM (Extension Module) which is a hardware unit. However this relation could be changed by the application program, in an RP2/RP4, by writing a new value to the EM address register.

2.2 General RPD family

RPD is a family of processors that includes several processors with a standardized user call interface toward the operating system.

The members of the family are:

- a** RPD
One board processor with extended processor bus
- b** RPG
One board processor, placed in BYB 202 magazine, with Group Switch (DL2) Interface and connected to the RPB-P.
- c** RPG2
A processor, placed in BYB 501 magazine, with Group Switch (DL2) Interface and connected to the RPB-S.

The signal interface between the central software in RPS and the different members of the RPD family is almost the same as the signal interface between the central software in RPS and the RP2.

The most characteristic for the members of RPD family is the lack of the EM bus. Instead the application programs can communicate with external equipment through special hardware on the board or through application hardware connected directly to the processor bus. The RPD-member's processor bus can be extended to one or several other boards via the backplane. The way the communication will be performed is dependent on the member in the family.

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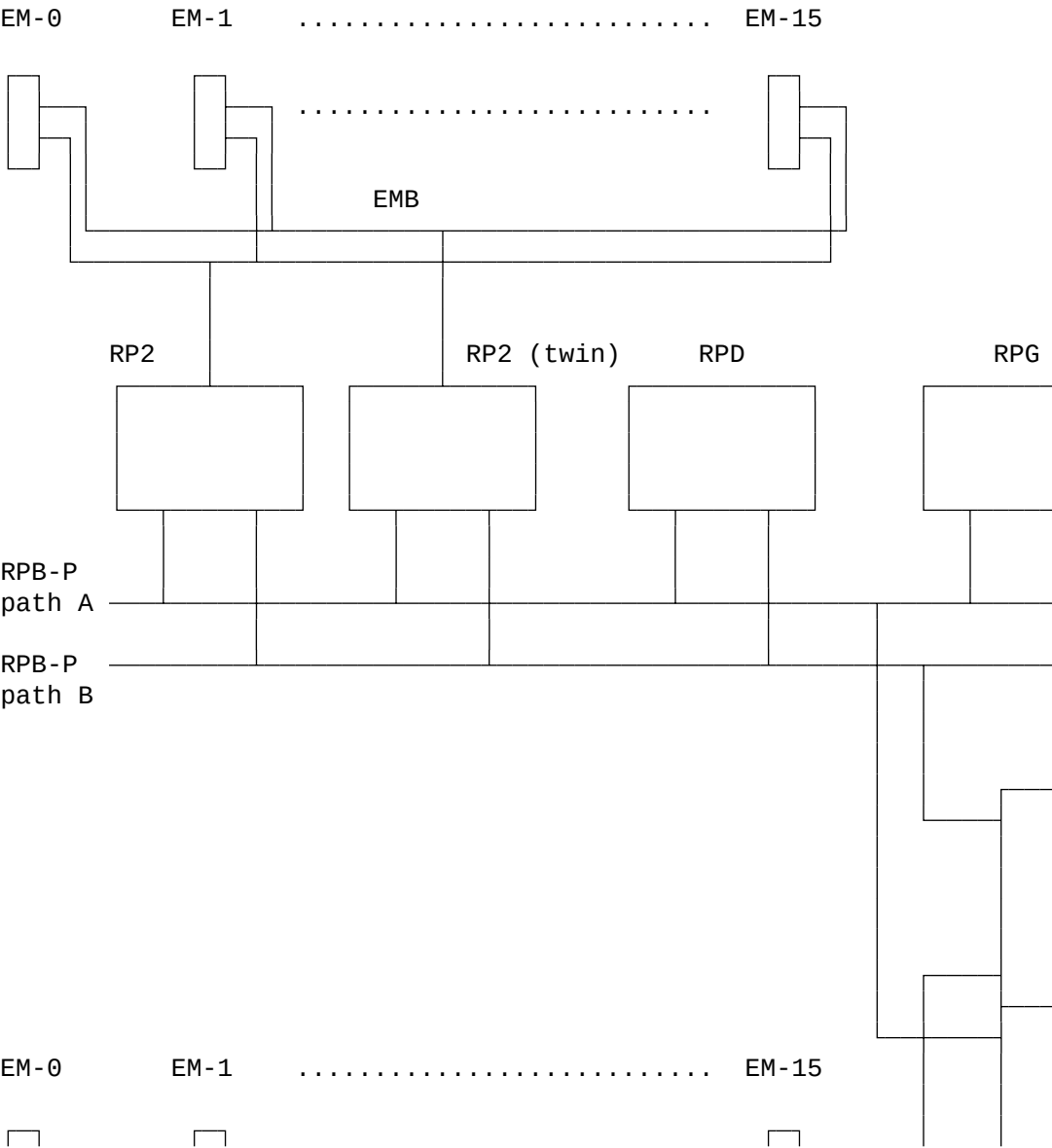
The members of the RPD family are designed for single control of application only. Duplication of RPD or RPG/RPG2 is not possible.

All interwork between CP and RPD/RPG/RPG2 is carried out through the transmission of messages, signals, over the Regional Processor Bus, RPB.

The addressing of signals from CP to the regional software units in RPD/RPG/RPG2 is defined by the RP-address and the CM (Control Module) number. An application unit loaded to the members of the RPD family can only be instantiated to just one CM.

No interwork takes place between different RPs.

Interwork between regional software units within the same processor is possible and is handled by the operating system in the different members of RPD family.



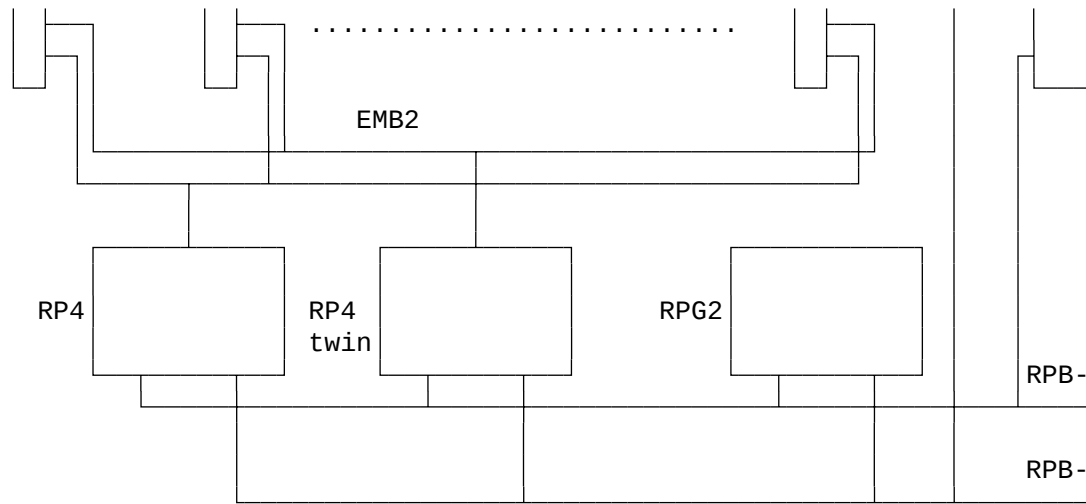


Figure 1. Bus connections for the RP2 and the RPD family

3 **Function**

3.1 **Survey**

The functions for program execution and data processing in the RP2/RP4 are implemented in regional software and hardware.

These functions are described in section 3.4.1 EXECUTIVE AND PROCESSOR FUNCTIONS IN THE RP2 FAMILY.

The functions for program execution and data processing in the RPD/RPG/RPG2 are implemented in regional software and hardware.

These functions are described in section 3.4.2 EXECUTIVE AND PROCESSOR FUNCTIONS IN THE RPD FAMILY.

The support functions in subsystem RPS-2 are implemented in central software, in regional software, in hardware and in microprogram.

The RP2/RP4 support functions are implemented in a central software, in a regional software, in a hardware and in a microprogram.

These are described in a section 3.2.1 SUPPORT FUNCTIONS IN THE RP2 FAMILY and they are:

Support functions - Program test

The RPD support functions are implemented in a central software, in a regional software, in a hardware and in a microprogram.

The RPG/RPG2 support functions are implemented in an regional software, in a hardware and in software running on a host computer.

These are described in a section 3.2.2 SUPPORT FUNCTIONS IN THE RPD FAMILY and they are:

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Support functions - Program test

The maintenance functions that are implemented in central software only are common for both RP2 and RPD families.

These are described in section 3.3.1 MAINTENANCE FUNCTIONS IN THE RP2 AND THE RPD FAMILY and they are:

Maintenance functions - Restart dump

The RP2/RP4 maintenance functions are implemented in regional software, in microprogram and in hardware.

These are described in section 3.3.2 MAINTENANCE FUNCTIONS IN THE RP2 FAMILY and they are:

Maintenance functions - Fault detection
- Magazine power supervision.

The RPD/RPG/RPG2 maintenance functions are implemented in regional software and in hardware.

These are described in section 3.3.3 MAINTENANCE FUNCTIONS IN THE RPD FAMILY and they are:

Maintenance functions - Fault detection

3.2 Support Functions

3.2.1 Support functions in the RP2 family

3.2.1.1 Program test

The program test function provides the capability to trace on instruction addresses, signal sending/reception, writing/reading to/from EM and to print out variable contents. This function is coordinated within the correspondent functions for CP, and also for EMRP. This means that cooperative supervision of the course of events can be done in different parts of the system.

The function is implemented with hardware (trace bits in the memory), microprograms, programs in RP and programs in CP.

Function blocks TERT, TERV and TERO

3.2.2 Support functions in the RPD family

3.2.2.1 Program test RPD member

A debugger on system level is supported.

The debugger comprises functions for monitoring processes and signals and for tracings on processes and signals.

The system debugger is a part of the Operating System and is available either through the RS232 ports, placed in the front of the RPD board, or from the Central Processor.

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Function block RDEX and TEDC (a part of RPS-B subsystem).

3.2.2.2 Program test RPG/RPG2 member

For fault finding purposes the operating system is equipped with three debugger levels. All levels are controlled by a debugger sited on a host computer. Connection to the operating system is made through the RS232 ports on the front of the RPG processor board.

Function block RGEX.

3.3 Maintenance Functions

3.3.1 Maintenance functions in the RP2 and the RPD family

3.3.1.1 Restart dump

If a fault occurs which causes a restart of RP, the contents of register, signal buffers, jump address storage and memory contents are read from RP and printed. The dump function can be made active or passive per RP by command.

The number of dump printouts both regarding the number of concerned RPs and the amount of data are limited.

Function blocks RPDU and RPDUD

3.3.2 Maintenance Functions in the RP2 family

3.3.2.1 Fault detection

A fault in RP2/RP4 is detected by means of routine tests in the RP, or by supervisory functions in RP2 family. Processor functions are tested routinely.

The routine tests are executed by the regional part of block RPFDD.

RPFDD belongs to regional processor subsystem RPS-B and is described there.

The program execution is supervised through time supervision (watchdog) and by checking unreasonable program and data addresses and illegal operation codes.

Parity supervision is carried out for the program and data store as well as for the microprogram memory. Supervision is performed only for those parts which are used.

Rapid fault detection is supported by microprogrammed sequences for example checksum calculations of the program memory.

When restarting the RP2 the bus interface circuit, BIC, can send an autonomous alarm signal to CP. This makes it possible for CP to analyse the fault even if normal signalling to or from RP does not work.

Function blocks CURP (RP2) RPHWM1 (RP4) and MIRP (RP2 and RP4).

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3.3.3 Maintenance Functions in the RPD family

3.3.3.1 Fault detection

A fault in RPD/RPG/RPG2 is detected by means of routine tests or by supervisory functions in the RP. Processor functions are tested routinely.

The routine tests are administered by the regional part of block RPFd and executed with help from the operating system and the processor hardware.

RPFd belongs to regional processor subsystem RPS-B and is described there.

The program execution is supervised through time supervision (watchdog) and by checking unreasonable program and data addresses and illegal operation codes.

Parity supervision is carried out for the program and data store. Supervision is performed only for those parts of the memory which are used. RPG's unused memory is however checked once a night.

At power-on the whole memory is always checked to avoid read/write errors during loading and execution of software. RPG/RPG2 also performs a check of unused memory once per night.

The bus interface circuit (BIC), in RPD and RPG, can send an autonomous alarm signal to CP. This makes it possible for CP to analyse the fault even if normal signalling to or from RP does not work.

Function blocks RPDHW, RDEX (RPD) and RPGHW (RPG), RPHWM2 (RPG2), RGEX (RPG and RPG2).

3.4 Executive and Processor Functions

3.4.1 Executive and Processor Functions in the RP2 family

3.4.1.1 Processor structure

A processor in RP2 family is an Ericsson designed 16-bit processor, in other words the memory, registers and arithmetic unit have a width of 16 bits. There are 14 processor registers. Some of them have special functions, but all registers can be used for reading, writing and arithmetic operations. In addition to the general registers, there is a link register stack for linked jumps and returns, and a jump address memory. All jumps are stored in the jump address memory which is used for fault tracing.

The hardware and microprogram of RP2/RP4 supports tracing on instruction address, data, EM bus and signals. When tracing takes place, an interrupt is made in the program execution and a jump is performed to a special program which stores the desired information. A trace bit in the memory is used for tracing on instructions and data. Other tracing operations are carried out with the aid of the microprogram.

Function blocks CURP (RP2), RPHWM1 (RP4) and MIRP (RP2 and RP4).

3.4.1.2 Addressing

The RP2 family has a read/write memory of 256 KW16, expandable to 512 KW16 (only in RP2). This memory is used for programs and data. In addition to this memory, there are separate address areas for read only memories and hardware addresses.

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Each program is allocated a certain space for programs and a certain space for data. Checks that addressing does not take place outside these areas are performed by microprogram and hardware.

All addressing of programs and data takes places relative to the start of each allocated area. This means that programs and data can be allocated freely.

Each control module (CM) can be maximum 64 KW16 of program and 64 KW16 of data.

Function blocks CURP (RP2), RPHW1 (RP4) MIRP (RP2 and RP4) and REX (RP2 and RP4).

3.4.1.3 Interface to EM bus

The application hardware is accessible with the EM bus. Special instructions are used to read and write in test and operation points respectively.

Function blocks involved CURP (RP2) and MIRP (RP2 and RP4).

3.4.1.4 Interface to RP bus

Signals are sent to and from CP via the RP bus. There are buffers in RP for 32 signals in each direction for this purpose. Each signal buffer size are 128 bytes. This means that the maximal data length of a signal is 125 bytes, signal head excluded.

Signal transmission to CP from a program in RP is carried out by calling the executive system. The signal is then fetched from the program's data area and placed in the output buffer. From there it is sent with special hardware. This is done when a signal fetching order arrives from CP.

When signal reception from CP takes place, the signal is first entered in the input buffer. When the signal call to the application program will be executed the signal is copied to the program's data area.

It is not possible to send signals to any other program in RP.

Function blocks involved CURP (RP2), RPHWM1(RP4) and MIRP(RP2 and RP4).

3.4.1.5 Monitor

A new primary interval starts every 5 milliseconds. The application programs are called in sequence at the start of this interval. When the application programs have been fully executed, the control system programs (e.g. programs for fault detection and test system) are called in the same way.

The program for fault detection always has access to a certain amount of time, even if the RP is overloaded.

Between each program call, a check is made to see if there are signals in the input buffer. If so, they are processed immediately. The signal is placed in the addressed program's data area and the program is called.

If there has not been time to execute all programs fully within 5 milliseconds, the primary interval will be extended. Consequently, no absolute time can be calculated in RP.

RP has only one priority level for programs.

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Function block REX.

3.4.1.6 Load regulation

When the output buffer to CP becomes half full (16 out of 32 signals), the calls of application programs every interval are stopped. These are resumed again when the number of signals in the output buffer has dropped to 8.

If the input buffer becomes filled, the RP stops sending acknowledgments on the RP bus. RPH in CP then attempts to resent the signal. If, within a certain length of time, sufficient space is not available for a further signal in the input buffer, the RP will be restarted.

Function block REX.

3.4.1.7 Load protection

The purpose of load protection is to avoid CP system restart caused by heavy signalling from RP during a time period of several minutes.

When the outbuffer for signals to CP in RP has reached a high level a signal is sent to CP. Simultaneously the application program is informed to stop the signalling to CP. Depending on the CP load the receiving program in CP sends an acknowledge to the RP. When this acknowledge is received the signalling to CP is resumed.

Function block REX.

3.4.1.8 Start and loading

Start or restart occurs after power up, on receipt of an order from CP or when a fault is detected. The bus senders in RP are then blocked. Signal buffers, jump address memories, processor registers and part of the executive system's variables are dumped and the executive program is copied from a read only memory, PROM and FLASH, by the microprogram in the RP2 respectively in the RP4.

A maintenance program in CP (block RPREC see description of regional processor subsystem RPS-B) orders a check to see if the programs in the read/write memory have the correct checksum. This checksum test is executed by the REXR. If any of the programs in the read/write memory have an incorrect checksum then reloading of all programs take place (block LARP see description of regional processor subsystem RPS-B). A CP-stored version is then, in the case of an incorrect checksum in the read/write memory, loaded in the RP by LARP in cooperation with the read only memory version of the executive program.

It is thus the CP-loaded version which normally executes. This makes it possible to release new versions of REX without hardware changes.

Note that if the read only memory version of REX is the current one there is no need for a CP stored version.

All programs which are executed in RP2/RP4 are stored in the read/write memory. Normally they are loaded from CP. There is, however, also a possibility of having the application program stored in read only memory in the RP. In this case they are always copied from read only memory at each restart. This feature is only intended for use in those cases an RP program must work before the maintenance and support functions in CP has become active.

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Function blocks involved CURP(RP2), RPHWM1(RP4) and MIRP(RP2 and RP4).

3.4.2 Executive and Processor Functions in RPD family

3.4.2.1 Processor structure

In the following description the members of the family are denoted with the acronym RPD respective RPG and RPG2. The RPD member is built on the HW platform PRO20 in HW block RPDHW and with the operating system RDEX.

The RPG and RPG2 members are built on the HW platform PRO60GS in HW block RPGHW respectively RPHWM2 and with the operating system RGEX.

The members of the RPD family has a 32-bit processor, in other words the memory, registers and arithmetic unit have a width of 32 bits. All of the process registers can be used for reading, writing and for arithmetic operations.

RPD has in addition to the general registers a jump address memory where the last 32 jumps are stored.

Function block RPDHW (RPD), RPGHW (RPG) and RPHWM2 (RPG2).

3.4.2.2 Addressing in RPD member

RPD member exists in two versions with a read/write memory of 4 MW8 respective 16 MW8 and an address space of 256 MW8. The read/write memory is used for programs and data. In addition to this memory, there are separate address areas for read only memory and hardware addresses.

Each program is allocated a certain space for programs and a certain space for data. Checks that addressing does not take place outside these areas are performed by special hardware.

All programs are generated with instructions and data addresses from zero. Programs and data are then relocated to their absolute addresses during start and restart. In other words all memory references in the program code are recalculated to correspond to their absolute location in the memory where they are loaded. This means that programs and data can be allocated freely.

Dynamic data for processes and signals are allocated from memory pools.

The maximum allowed program volume is 2 MW8.

For each program there is no limitation of the size of DS that can be used except for the total available memory space.

Function block RDEX and RPDHW

3.4.2.3 Addressing in RPG and RPG2 member

Each program is allocated a certain space for programs and a certain space for data. Checks that addressing does not take place outside these areas are performed by the Memory Management Unit (MMU) in the microprocessor hardware.

The total physical memory size is 16 MW8. The board is prepared for later expansion up to maximum 64 MW8.

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The logical address space is 4 GW8. For debugging reason it is supposed that application programs are allocated to unique absolute addresses within the logical address space. If a program is allocated to an already occupied logical address space, the operating system will automatically relocate the program to a new address space. The memory management unit (MMU) makes the translation from logical to physical addresses every time a address reference occur.

Dynamic data for processes and signals are allocated from memory pools. The pools are configurable by the applications.

The maximum allowed program volume is 2 MW8.

For each program there is no limitation of the size of DS that can be used except for the total available memory space.

Function block RGEX, RPGHW (RPG) and RPHWM2 (RPG2).

3.4.2.5 Interface to Hardware in RPD member

The application hardware is connected directly to the internal RP processor bus. The application programs has high priority to and fast access to the processor and its resources, such as interrupt service routine execution, without involving the executive program RDEX.

RDEXR is however used to insert user defined Interrupt Requests (IRQ's).

Function blocks involved RPDHW and RDEX

3.4.2.6 Interface to group switch in RPG and RPG2 member

RPG/RPG2 are designed for applications that communicate with the external equipment through an integrated group switch interface, DL2. The interface supports two different protocols, LAPD and the Signalling System #7.

The application can, by means of signals, open and close channels and specify the configuration of each individual channel.

For special applications, the SNT/DL2 interface hardware can directly be controlled by the application programs.

3.4.2.7 Interface to RP bus in RPD family

Signals are sent to and from CP via the RP bus. There are 512 signal buffers in each direction for this purpose. Each signal buffer size are 64 bytes. This means that the maximal data length of a signal is 61 bytes, signal head excluded.

Signal transmission to CP from a program in RP is carried out with the aid of signal sending to the executive system. When the executive system block RDEX/RGEX then receives a signal from a user RDEX/RGEX places the signal in the TX-buffer, which is a buffer for RP signals that is to be transmitted to CP. From there it is sent with special hardware. This is done when a signal fetching order arrives from CP.

When signal reception from CP takes place, the signal is first entered in the RX-buffer, which is a buffer for RP signals which are received from CP.

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The executive system RDEX/RGEX then fetches the signal from the RX-buffer and checks if the addressee is found in its table of processes and blocks. If so RDEX/RGEX then transfers the signal to the addressee.

Function blocks involved RDEX/RGEX and RPDHW/RPGHW/RPHWM2.

3.4.2.8

Executive Functions in RPD family

The executive system can work in either active or passive mode. Only a limited number of functions can be used in the passive mode. The executive functions for RPD family include process administration, signal handling, timer handling, bus handling, service routines, and handling at switch-on of power.

Processor administration

The executive system contains routines to create and kill processes.

A process can have one of 16 priorities, the lower priorities implement a time-sharing environment in which processes are pre-empted after a certain time slice.

The executive administers the saving and restoring of a process context.

Signal handling

The executive system handles signals between the application processes. The executive system can also handle signals to and from CP (see item INTERFACE TO RP BUS IN RPD FAMILY).

Bus handling

For interwork towards the bus RPB, that is connected to RPD/RPG/RPG2, the executive include functions for transmission and reception of signals (see item INTERFACE TO RP BUS IN RPD FAMILY).

Timer handling

The executive provides functions for sending of signals with a specified delay, it is also possible to read the absolute time.

Service routines

The executive system contains certain routines that handles requests for connecting a hardware interrupt with a user routine, request information on memory allocation, etc.

The service routines are called by the application processes with signals.

Switch-on power

When power is switched on a hardware check is performed and the executive system enters passive mode.

Function block RDEX/RGEX

3.4.2.9

Start and loading

Start or restart occurs after power up, on receipt of an order from CP or when a fault is detected. The bus senders in RP are then blocked.

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The part of the executive program which works in passive mode is copied from a non volatile memory at power on and at restart caused by errors. A maintenance program in CP (block RPREC and RPRES see description of regional processor subsystem RPS-B) orders a check to see if the programs in the read/write memory have the correct checksum.

This checksum test is executed by the part of the operating system which has been copied from the read only memory to RAM.

If any of the programs in the read/write memory have an incorrect checksum then a complete reload of all program takes place (block LARP see description of regional processor subsystem RPS-B).

All programs which are executed are stored in the read/write memory.

Function blocks involved RDEX/RGEX

3.4.2.10 Test support in RPD member

The RPD is equipped with an embedded system level debugger. The debugger can be reached through one of the RS232 asynchronous serial ports on the board front or by initiating a debugger path with a command to establish a path between the IO device and the RPD level debugger. When the path is opened, the operator works in a dialogue mode and can use the RPD system level debugger commands.

The command receiving block, TEDC, belongs to subsystem RPS-B and is described there.

All trace conditions will remain after a CP restart but not a RP restart. The debugger path however does not remain after a system restart.

Tracing on variables and program addresses can only be executed with the aid of the special development environment used for the executive system through a direct connection on the processor board.

3.4.2.11 Test support in RPG and RPG2 member

The RPG/RPG2 are equipped with an embedded monitor for source level debugging. The debugger itself runs on a host computer and communicates with the monitor via one of the RS232 asynchronous serial ports on the board front. The debugger can be run in two modes.

In the first mode the debugger takes over the entire target. That means when the program runs into a break-point all executing are stopped and the debugger waits for next command to enable examination of variables and registers. This debugger mode is available independent of what mode the target processor is running in.

The middle level debugger level can only be entered when the RPG/RPG2 is running in active mode. In this case the debugger is aware of processes so running into a breakpoint will only stop the actual process while the remaining processes are still running. The variables of the stopped process can then be examined.

The RPG/RPG2 is also equipped with a system level debugger. With the highest debugger level trace of signals and processes can be done. The command interpreter and presentation routine are run on a host computer

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and communicates with the monitor via one of the RS232 asynchronous serial ports on the board front.

To be able to use these debugging features completely it is possible to run RPG/RPG2 without central processor support. The RPG/RPG2 is then loaded from a host computer via the RS232 serial port and also fed with signals the same way.

Function block RGEX.

4 Function Blocks

4.1 Support Functions in CP

4.1.1 Support Functions in RP2 family

4.1.1.1 TERT, Program testing, Tracing functions

This block analyses and executes the commands for defining/ re-defining and activating/passivating watchdogs and actions in RP.

The block receives tracing information in RP and forwards it to block TERO.

TERT is subdivided into a central and a regional part.

4.1.1.2 TERV, Program testing, Variable-handling functions

TERV receives commands concerning variables and memory information. The block reads and prints out the desired information.

4.1.1.3 TERO, Program testing, Printout functions

This block receives tracing information from RP and stores it in central PTS tracing memories for later printout. TERO prints out information on RP tracings which have occurred after receipt of an order from central PTS.

4.2 Maintenance Functions in CP

4.2.1 Maintenance functions RP2 and RPD

4.2.1.1 RPDU, Dump handling RP

Dump information from RP, printout routines and commands for activating, passivating and printing of memory. The dump information are handled in RPDU.

4.2.1.2 RPDUD, Dump handling RPD family

Dump information from RPD/RPG/RPG2, printout routines and commands for activating, passivating and printing of memory. The dump information are handled in RPDUD.

4.3 Executive and Processor Function blocks

4.3.1 Executive and Processor Function blocks for RP2 family

4.3.1.1 REX, executive system

REX is the executive program in the RP2/RP4. It consists of two parts: REXR and REXU.

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REXR is the regional executive program and REXU is the central situated program unit. REXU and REXR cooperate to protect CP from overload of signals from RPs.

A monitor in REX deals with:

- a** -
Recalling deblocked CMs every primary interval.
- b** -
Recalling CMs when signals arrive from CP.

CP can carry out the following operations by means of signals to REX:

- a** -
Block/deblock the RPs bus senders. Blocking of the bus senders implies loading of programs from Read Only Memory
- a** -
Execute a soft restart of the RP2/RP4, which includes the following actions: a) stop call of application programs b) passivate tracing c) clear DS for application programs
- b** -
Fetch restart information.
- c** -
Set state for RP and EM bus.
- d** -
Make checksum calculation of programs in RP.
- e** -
Load out program.
- f** -
Link CMs to programs.
- g** -
Block/deblock CMs.
- h** -
Test supervisory circuits.
- i** -
Echo-test RP.

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- j** -
Read/write in RP memory.

Programs in RP can carry out the following operations by means of executive system calls:

- a** -
Sends signals on RP bus.
- b** -
Obtain information on program and data allocation.
- c** -
Link CMs to programs.
- d** -
Mark and activate tracings.

4.3.1.2 **MIRP, microprogram**

The microprogram contains functions for restarts, interrupt handling and instruction execution.

The instructions which are executed consist of read and write instructions to memory, arithmetic operations and jump instructions, of a type which are included in normal program execution. MIRP also contains special instructions for maintenance programs, test systems and executive systems. These include instructions for checksumming program stores, for memory tests and processor tests.

Parts of the microprogram are also executed in connection with an interrupt or restart.

The fault supervision is shared by the microprogram and hardware. Examples of fault supervision actions carried out by the microprogram are checks of data addresses (not program addresses) and checks of undefined operation codes.

4.3.1.3 **CURP, RP2 hardware**

The hardware for RP2 is completely implemented in block CURP. CURP consists of magazine RPM6, circuit board EMBCB-F and EMBCB-H.

EMBCB-F/H boards makes it possible to allow the use of new modernized APT hardware (built in BYB 501) together with the RPB-P.

4.3.1.4 **RPHWM1, RP4 hardware**

The hardware for RP4 is implemented in block RPHWM1. RPHWM1 consists of plug-in units RP4-F and RP4-H.

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4.3.2 Executive and Processor Functions in RPD family

4.3.2.1 RDEX, executive system

RDEX is the executive program in the RPD member.

It consists of two parts: RDEXR and RDEXPR. RDEXR and RDEXPR are built on the OSE Classic real time kernel for the 68020 CPU.

RDEXR is the complete operating system for execution of application programs. It executes when the executive system works in active mode.

RDEXPR executes when the executive system works in passive mode. Only a limited number of functions can be executed in passive mode like answering echo signals and handling of program loading.

RDEX contains functions which are executed when the following events occur:

- a** -
When a signal from CP is received in the RPD.
- b** -
When a signal is sent from the RPD to be received in CP.
- c** -
When a signal from a user program within the RPD is received in RDEX.
- d** -
When a signal sent from RDEX is received in a user block within the RPD.
- e** -
When a call from a HW handler within the RPD is received in RDEX.
- f** -
When a call from RDEX is received in a HW handler within the RPD.
- g** -
When a system call from a user program within the RPD is received in RDEX.

The CP can, with signals to the RPD:

- a** -
Block and deblock the bus senders in the RPD.
- b** -

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Execute a soft restart of the RPD, which includes the following actions:

Order to application programs to stop sending signals to CP

Abort of all signals within the RPD;

c

-

Set the state of the RPD.

d

-

Calculate checksums for the programs in the RPD.

e

-

Block and unblock CMs.

f

-

Test supervision circuits.

g

-

Perform echo tests on the RPD.

h

-

Perform CPU load measurements in the RPD.

i

-

Perform Read and write tests in the RPD memory.

The RPD can with signals to the CP:

a

-

Send autonomously error reports from BIC to CP.

b

-

Transfer a signal from CP-User or from User-CP.

User programs can with signals to the RPD:

a

-

Install interrupt vectors.

b

-

Fetch program and data allocation information.

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- c** -
- Fetch the address of a User's program memory
(Only initiated from the regional part of RPFDR).
- d** -
- Fetch the address of a User's data memory.
(Only initiated from the regional part of RPFDR).

The RPD can with signals to a User:

- a** -
- Start a User.
- b** -
- Block and unblock a User.
- c** -
- Start and stop a User to minimize the CP load.

The hardware device can by calling the RDEX:

- a** -
- Report errors to RDEX.
- b** -
- Call the RDEX timer routine.
- c** -
- Call the RDEX sleep routine.
- d** -
- Call the RDEX wake up routine.
- e** -
- Start RDEX at boot.

The RDEX can by calling the hardware devices:

- a** -
- Initiate the RP bus.

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- b** -
Read and write in a buffer from the CP.
- c** -
Initiate the RS232-port.
- d** -
Read and write characters on the RS232-port.
- e** -
Initiate the timer.
- f** -
Read and write the state of the RP bus.
- g** -
Initiate the watchdog.
- h** -
Read the BIC buffer state.
- i** -
Initiate interrupt processes.
- j** -
Initiate restart caused by an error.

User programs can with system calls:

- a** -
Send and receive signals on the RP bus.
- b** -
Delay signals.
- c** -
Change priority.
- d** -
Fetch own and other processes' identity.
- e** -
Create and kill processes.
- f** -

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Fetch buffers from and return buffers to the OS.

g

-

Get the present time from the OS.

4.3.2.2 RGEX, executive system

RGEX is the executive program in the RPG/RPG2 member.

It consists of five parts: RGEXR, RGEXM, RGEXB, RGEXH and RGEXP. RGEXP and RGEXR are built on the OSE Delta real time kernel for the Motorola 68060 CPU.

RGEXR executes when the executive system works in active mode.

RGEXP executes when the executive system works in passive mode. Only a limited number of functions can be executed in passive mode.

RGEXB executes at power on. It also contains some low level functions used by RGEXP. The behaviour of RGEXB is monitored by inserting a test plug on the board front. By the test plug it is possible to force RGEXB to wait for commands via one of the RS232 serial ports.

RGEXM is a monitor used when debugging the programs loaded to the RPG.

RGEXH is used for on line help for RGEXB.

With commands it is possible to:

a

-

List possible commands (HELP)

b

-

Set new/change parameters

c

-

Load programs to RAM

d

-

Save program/parameter in FLASH

e

-

Remove program/parameter from RAM

f

-

Run program

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The first thing RGEXB does after power on is to find out if the HW works by running a simple HW check. If the hardware is found to be correct the requested program is copied from FLASH to RAM and started. In the normal boot procedure without any test plug inserted the program for secondary boot phase, RGEXP, is copied to RAM and is started.

The behaviour of RGEX both in passive and active mode is the same as for RDEX in RPD.

4.3.2.3 RPDHW, hardware

The function block RPDHW implements hardware functions for regional processor control of APZ and APT equipment in AXE.

The magazine for the RPD contains hardware both for APZ and APT.

The processor unit is called RPD.

The hardware for the RPD is completely implemented in block RPDHW and consists of units (circuit boards) PRO20 and RPBU.

Depending on which application uses the services of the processor, different application hardware is connected directly to the internal processor bus.

One example of application hardware is the TRH (Transceiver Handler) board.

The magazine containing the RPD boards and the application hardware board is then called TRHM.

4.3.2.4 RPGHW, hardware

The function block RPGHW implements hardware functions for regional processor control of APZ and APT in AXE. The RPG is in first hand intended to be used by applications that needs an SNT/DL2 interface. The hardware board is completely equipped for that purpose. No extra application hardware is possible to connect.

The processor unit is called RPG.

The hardware for the RPG is completely implemented in block RPGHW and consists of units (circuit boards) PRO60GS, RPBU and magazine RPGM.

4.3.2.5 RPHWM2, hardware

The function block RPHWM2 implements hardware functions for regional processor control of APZ and APT in an modernized AXE (equipment practice BYB 501). The RPG2 is in first hand intended to be used by applications that needs an SNT/DL2 interface. The hardware board is completely equipped for that purpose. No extra application hardware is possible to connect.

The processor unit is called RPG2.

The hardware for the RPG2 is implemented as a plug-in unit which consists of a motherboard and a daughterboard.

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5 Hardware

5.1 Hardware in RP2

5.1.1 Overview

The RP2 is a processor designed in the first place to be compatible with the old RP in an AXE system, RP1. This means that it has the same bus interfaces - RP Bus and EM Bus - identical to RP1 and that all RP1 instructions can be emulated on RP2.

RP2 has an internal structure that is similar to a standard microprocessor. Still, because it is microprogrammed, it can achieve a high capacity for very specialized tasks.

There are four memories included in RP2:

one read/write memory (DRAM) for programs and data,

one read only memory for programs,

one read only memory for microprograms and

one read/write memory for process registers and jump address storage.

The processor logic in RP2 consists of 3 main parts:

The address handler, the data handler and the arithmetic and logic unit.

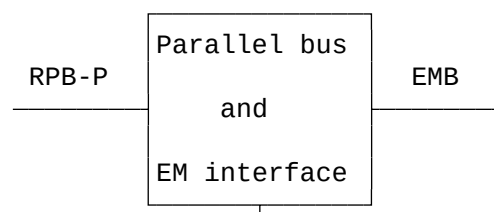
The address handler calculates the addresses to the main store for program and data, and provides DRAM refresh.

The data handler supports data transports to and from the main memory. Prefetch registers, situated in the data handler, where the two following program words are stored, permit a rapid execution of very short instructions. Most of the logic is implemented in customer designed circuits.

The arithmetic unit is the hardware to perform instruction execution. The address handler, the data handler and the arithmetic unit forms together with the microprogram the processor unit.

There are three buses in the RP2 that connect the logic units and the memories. Data transports can be made simultaneously on all three buses.

Bus interfaces, implemented in a BIC, handle the communication to and from CP and to and from EMS.



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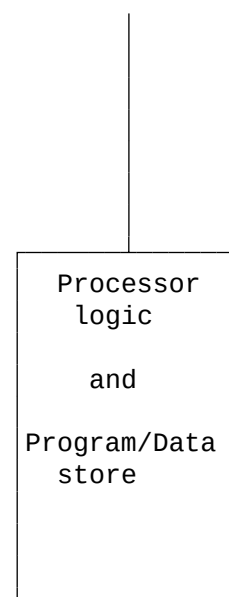


Figure 2. Hardware Survey for RP2

5.1.2 Functions

5.1.2.1 Test support

There are two types of test support. One consists of support for tests during operation and the other of support for basic testing of the RP with connected hardware. The first is described in section 3.3.2.1. In the basic testing case, a control board is connected to the board front of RP. It can be used for stepping instructions, stopping at program addresses and reading or writing in the read/write memories. The processor contains hardware which supports these functions.

5.1.2.2 Handling RPB and EMB

The processor contains a protocol circuit, BIC, for signalling on RPB and EMB. When signals are received or sent on RPB, BIC transfers the entire signal autonomously to or from the signal buffers in main store in the RP. This occurs on orders from the RPH (Regional Processor Handler) in CP. Between individual signals on RPB, BIC receives new signal buffer addresses by interrupting the processor's program execution.

When data transfer take place on EMB, the microprograms controls the exchange of data directly on the 4-bit or 8-bit level.

5.1.2.3 Supervisory functions

Hardware supervises parity both in the memory for programs and data and in the microprogram memory. There is also a function for supervising the execution time for programs (watchdog). This function causes an interrupt if the execution time for a program is too long, for example if an infinite loop occurs.

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Hardware checks also ensure that addressing above the limit can not take place for the program area. (The corresponding checks for the data area is performed by microprogram.)

5.1.2.4 Autonomous error signals

A function is provided for autonomous error signal transmission in BIC to permit a more rapid fault detection and better fault indication. This function minimizes the cases in were RP is regarded faulty with no other fault indication than the fact there is no reply to an echo test. When transmitting the signal, no memory in RP is utilized. Only BIC and the interface to RPB need be serviceable.

The function can be initiated by three hardware signals to BIC and can be also started by means of software.

The error signal inputs used are as follows:

- a** -
Parity error in memory. Initiated by HW.
- b** -
Parity error in microprogram. Initiated by HW.
- c** -
Execution time supervision detected error. Initiated by HW.
- d** -
Program detected error. The signal is initiated by software.

5.1.2.5 Blocking of senders to RPB.

BIC has an autonomous function for blocking its bus senders to RPB. This function exists to be able to protect the signal interwork on RPB when an individual RP illegally sends on RPB. The function, which works completely independent of the processor function, blocks/deblocks the senders on receipt of special order codes from CP via RPB.

5.1.3 Physical structure

The magazine containing the RP2 boards is called RPM6. See figure 3.

RPM6

R	P	R
P	R	P
B	O	B
U	/	U
	M	
	E	
	R	
	/	
	P	

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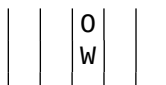


Figure 3. Magazine layout for RPM6.

The RP2 processor consists of two types boards:

a RPK

This board is the processor board. It contains the processor circuits, memory, power unit and the Bus Interface Circuit (BIC). The BIC handles both the RP bus and the EM bus (EMB). The EM bus is connected on the front of this board.

b RPBU

contains the electrical interface towards the RP bus (RPB). It converts the TTL-level signals on the processor board to AC-coupled signals on the RP-bus, using transformers. The RP bus is connected to the front of the RPBU board. Each RPBU is connected to it's own CP side.

5.2 Hardware in RP4

5.2.1 Overview of RP4

RP4 is a plug-in unit which has same functionality as RP2, regarding RPB and EMB interfaces, but is designed for use in equipment practice BYB 501. The HW units are based on RP2 from the function block CURP.

From an application point of view RP4 and RP2 are binary code compatible.

RP4 is implemented as RP4-H (Half height) and RP4-F (Full height) board.

RP4-H/F board is divided in several function blocks, see fig. 4:

- RP block.
- Serial RP-bus repeater.
- Serial bus protocol handler.
- EMB2 handler.
- Maintenance bus master.
- Maintenance bus slave.
- Power supply connection and filter for the magazine.
- Redundant power supply for board.
- -48V voltage supervision.

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- RP-type info which indicates whether the RP is RP4-H or RP4-F.

RP4-H/F has following interfaces:

- A dual serial RP-bus Interface (RPB-S).
- EMB2 interface towards backplane and front (only in RP4-F).
- Power filter and backplane -48V distribution.
- Maintenance bus interface, master and slave.
- A dual -48V power supply.
- JTAG interface.

The RP block performs execution of instructions, supports calculation of addresses to the data and the program store, provides the DRAM refresh and supports data transfer to/from the main memory and contributes to an execution platform for application programs.

The RP block consists of 6 main parts: a processor (named RPC2), DRAM, PROM, clock circuits, power up reset circuits and glue logic in PLD (named GLC).

The serial bus repeater distributes the RPB-S to the next magazine. A buffer distributes the RPB-S to the backplane.

The serial bus interface takes care about signals from and to CP.

The interface consists of HDLC-controller circuit, SRAM for the controller and a Serial Bus Interface Circuit (SBIC).

SBIC implements special functions for the RPB-S, for example addressing, polling, clock regeneration, bus path control.

EM boards, placed in a GDM magazine, are connected to the RP4-H/F via an internal EMB2 in the backplane. In the RP4-F the bus, split into two branches, is also available in the front of the board.

RP4-H/F acts as a master and supplies, through the backplane, boards in a same magazine with a M-bus. As other boards, located in the same magazine, the RP4-H/F acts also as a slave on the other RP4-H/F maintenance bus.

Power, -48V, is connected to a connector on the RP4-H/F's front and distributed to the backplane through a power supply filter. From the backplane the doubled power supply is connected to the RP4-H/F. On the board it is converted, by doubled DC/DC converters, to +3.3V and +5.0V.

The power supply supervision of two power branches in the backplane is performed in each RP4-H/F.

RP4 can support the CP with its product individual data such as: product number, revision, name of the board, manufacturing date and a serial number.

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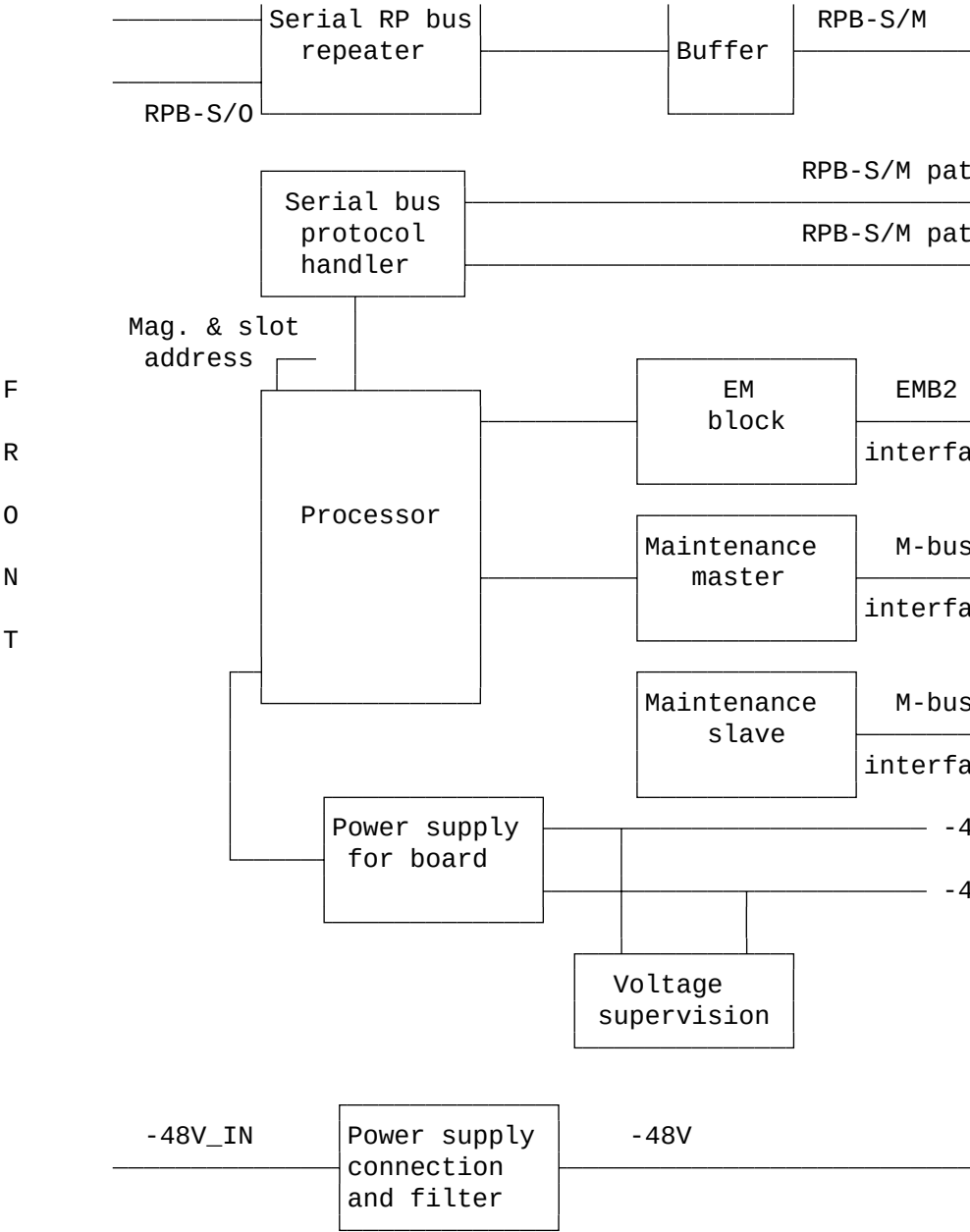


Figure 4. Hardware Survey for RP4-H/F

5.2.2 Functions

5.2.2.1 Production test support

- Test pads.

5.2.2.2 Handling of RPB-S, EMB2 and Maintenance bus

The buffer part in RP4-H supplies other RP-boards in the same magazine with a RPB-S connection through the backplane, RPB-S/M.

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The repeater supplies the next magazine on the RPB branch with a RPB-S connection through a frontpanel connector, RPB-S/O.

The RP part in RP4 uses an internal redundant RPB-S/M, path A and B, through the backplane. The RP also uses physical RP addresses, magazine and slot address, through the backplane. The repeater part in RP4-H uses RPB-S/I from an other magazine or the RPH through a frontpanel connector. It can, in addition to that, also supply the twin RP, if it is in an other magazine, with a RPB-S connection through an other frontpanel connector, RPB-S/X.

RP4-H distributes the EMB2 only to the backplane. For signal transmission reason the EMB2 is split in two branches. Each branch can handle half a magazine (max 8 EMs). The EMs are also connected to the RP-twin.

RP4-F distributes the EMB2 both to the backplane and to two front connectors. The bus is split as well and each branch handles half a magazine, max 8 EMs.

RP4 acts as a master on the M-bus and supplies boards in the same magazine with an M-bus connection through the backplane. All slaves on the bus are controlled by the master.

The M-bus is used for maintenance purposes of HW in the BYB 501 for example:

- During production different individual data can be written, through the M-bus, into a PROM.

On request from CP the individual data can be fetched from the PROM.

- LED, placed on the front of the board for indication of a manuel intervention, can be turn on/off.

As other boards the RP4 also implements a slave, connected through the backplane, on the other RP4-H/F maintenance bus, .

5.2.2.3 Supervisory functions in processor

Following supervision functions are implemented in RP4-H/F:

- Address limit supervision, data store.
- Address limit supervision, program store.
- Parity supervision.
- Watch dog.
- Voltage supervision for the internal board supply.

5.2.2.4 Power supply supervision

Both power supply branches, -48V-A and -48V-B, from the backplane are supervised by voltage comparators. The incoming voltage from the front to -48V filter is not monitored at all.



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- handling of the interface towards RPB
- handling of addresses
- handling of data
- handling of arithmetical and logical operations

The address handling function and data handling function is implemented in a customer designed circuit called CSC (CPU Support Circuit).

CSC calculates the addresses to the main store for program and data, and provides DRAM refresh. The circuit also includes parity checking and address boundary checks.

The data handler function supports data transports to and from the main memory. Instruction pre-fetch permits a rapid execution of short instructions.

The RPB interface function is implemented in a customer designed circuit called BIC (Buffer Interface Circuit).

The processor bus RPDBB (RPD Backplane Bus) defines the interface between the processor board and other units, which interwork with the processor for example application hardware.

The address handler function, the data handler function, and the arithmetic and logical operation function form the processor unit.

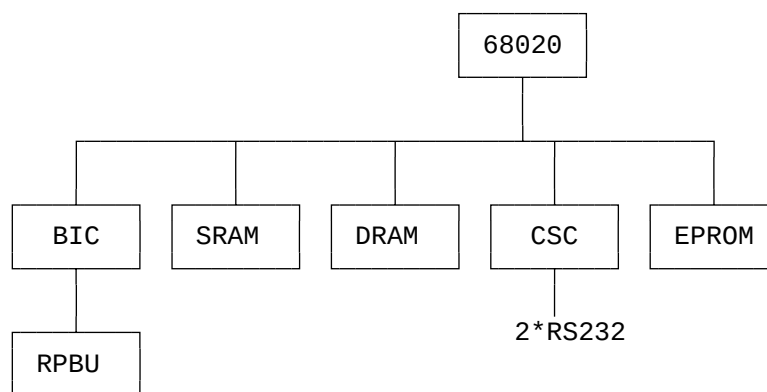


Figure 7. Hardware Survey for RPD

5.3.2 Functions

5.3.2.1 Handling RPB

The processor contains a protocol circuit, BIC, for signalling on RPB. When signals are received or sent on RPB, BIC transfers the entire signal autonomously to or from the main store. This occurs on orders from the RPH (Regional Processor Handler) in CP. Between individual signals on RPB, BIC receives new signal buffer addresses by interrupting the processor's program execution.

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5.3.2.2 Supervisory functions

Hardware supervises parity in the memory for programs and data. Supervising of the execution time for programs (watchdog). The watchdog causes an interrupt if the execution time for a program is too long, for example if an infinite loop occurs.

Hardware also checks ensure that addressing above the limit can not take place for the program area and for the data area.

5.3.2.3 Autonomous error signals

A function is provided for autonomous error signal transmission in BIC to permit a more rapid fault detection and better fault indication. This function minimizes the cases where an RP is regarded faulty with no other fault indication than the fact that there is no reply to an echo test signal from CP.

When transmitting the error signal, no memory in RP is utilized. That implies that only BIC and the interface to RPB need to be in service.

The function can be initiated by two hardware signals to BIC and can be also started by means of software.

5.3.2.4 Blocking of bus senders to RPB

BIC has an autonomous function for blocking bus senders to RPB. This function exists to be able to protect the signal interwork on RPB when an individual RP illegally sends on RPB. The function, which works completely independent of the processor function, blocks/deblocks the senders on receipt of special order codes from CP via RPB.

5.3.3 Physical structure

A typical application magazine for the RPD contains hardware both for APZ and APT.

Depending on which application uses the services of the processor, different application hardware is connected directly to the internal processor bus.

One example of application hardware is the TRH (Transceiver Handler) board. The magazine containing the RPD boards and the application hardware board is then called TRHM. See figure 8.

TRHM

P	R	P	R	T	P	R	P	R	T	P	R	P	R	T	P	R	P	R	T
O	P	R	P	R	O	P	R	P	R	O	P	R	P	R	O	P	R	P	R
W	B	O	B	H	W	B	O	B	H	W	B	O	B	H	W	B	O	B	H
E	U	2	U	B	E	U	2	U	B	E	U	2	U	B	E	U	2	U	B
R					R					R					R				

Figure 8. Example of magazine layout for TRHM.

Two different types of boards belonging to the RPD are used:

a RPBU

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contains the electrical interface towards the RP bus (RPB). It converts the TTL-level signals on the processor board to AC-coupled signals on the RP-bus, using transformers. The RP bus is connected to the front of the RPBU board. Each RPBU is connected to it's own CP side.

b PRO20

contains the following main parts:

- The main processor Motorola 68020
- A gate array circuit CSC (CPU Support Circuit)
- A gate array circuit BIC (Bus Interface Circuit)
- A dynamic RAM (DRAM) of size 1 MW32 or 4 MW32 depending of version of processor board.
- A static RAM (SRAM) of size 64 KW8
- An Erasable PROM (EPROM) of size 128 KW8
- An interface to the processor bus
- An Programmable Array Logic Device (PAL)

5.4 Hardware in RPG

5.4.1 Overview

The RPG member of the RPD family is designed for applications that has use of a SNT/DL2 interface. In the first place this interface is used for communication through the group switch.

The RPG is implemented with three printed boards. One board for the processor included power and the SNT/DL2 interface and two boards for the RPB connection.

The processor board contains a MC68060 CPU from Motorola that works in companion mode with QUICC32 (MC68360).

The QUICC32 circuit handles all communication via the RS232 ports and together with the GSNIC (Group Switch Network interface Circuit) constitutes the SNT/DL2 interface. QUICC32 also handles the addressing supervision and the timers.

The size of the DRAM (Dynamic Random Access Memory) is 16 MW8. The total address capacity is 4 GW8. Program code and data are stored in DRAM during normal program execution.

SRAM (Static Random Access Memory) is used for buffers to and from RPB/BIC. Signals from CP are stored in SRAM by BIC and later copied to DRAM by OS. FLASH memory contains boot procedures. By strapping the

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processor board in a special way it is possible to exchange programs and parameter data in the FLASH.

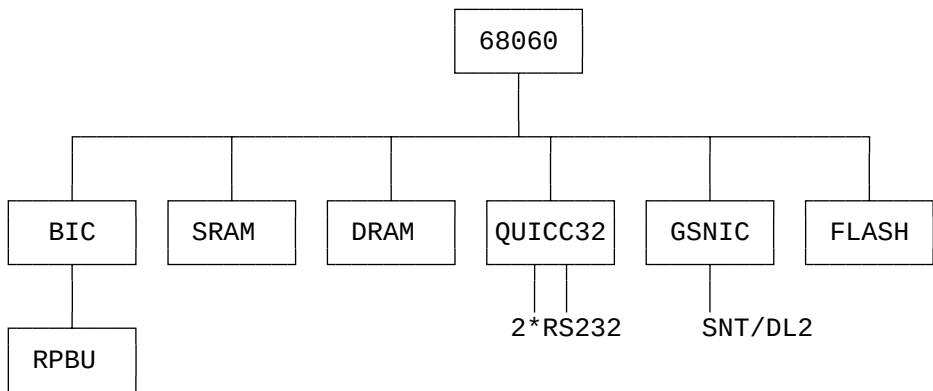


Figure 9. Hardware Survey for RPG

5.4.2 Functions

Supervisory functions.

Hardware supervises parity in the SRAM and DRAM memory. There is also a function for supervising the execution time for programs (watchdog). This function causes an interrupt if the execution time for a program is too long, for example if an infinite loop occurs.

Hardware also contains checks to ensure that addressing outside own program and data area boundaries not can take place.

5.4.3 Physical structure

A magazine for the RPG contains only APZ hardware.

RPG consists of three boards of two different types. For magazine see figure 10.

- a RPBU
 - contains the electrical interface towards the RP bus (RPB). It converts the TTL-level signals on the processor board to AC-coupled signals on the RP-bus, using transformers. The RP bus is connected to the front of the RPBU board. Each RPBU is connected to one CP side.
- b PRO60GS
 - The board contains the following main parts:
 - The main processor Motorola 68060
 - MC68360, QUad Integrated Communication Controller (QUICC32)

The QUICC32 circuit handles all communication via the RS232 ports, Ethernet ports and together with the GSNIC (Group Switch Network Interface Circuit) connects DL2B, available in the backplane, to the controller for further processing.

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The DL2B interface is connected to a DLHB board in the same magazine, which sends data over the DL3 interface to the Group Switch.

The size of the DRAM (Dynamic Random Access Memory) is 16 MW8. The total address capacity is 4 GW8. Program code and data are stored in DRAM during normal program execution.

SRAM (Static Random Access Memory) is used for storage of the microprogram for the HDLC controller for signals to/from the RPB-S.

The RPB-S is provided in the backplane from the RP4, which also provides -48V and the M-bus.

Following main functions are included in the RPG2.

- Power supply.
- Clock function.
- CPU.
- Reset function.
- Communications functions RS232.
- Communications functions Ethernet.
- Handling of the RPB-S.
- Handling of the DL2B.
- Maintenance bus, slave.

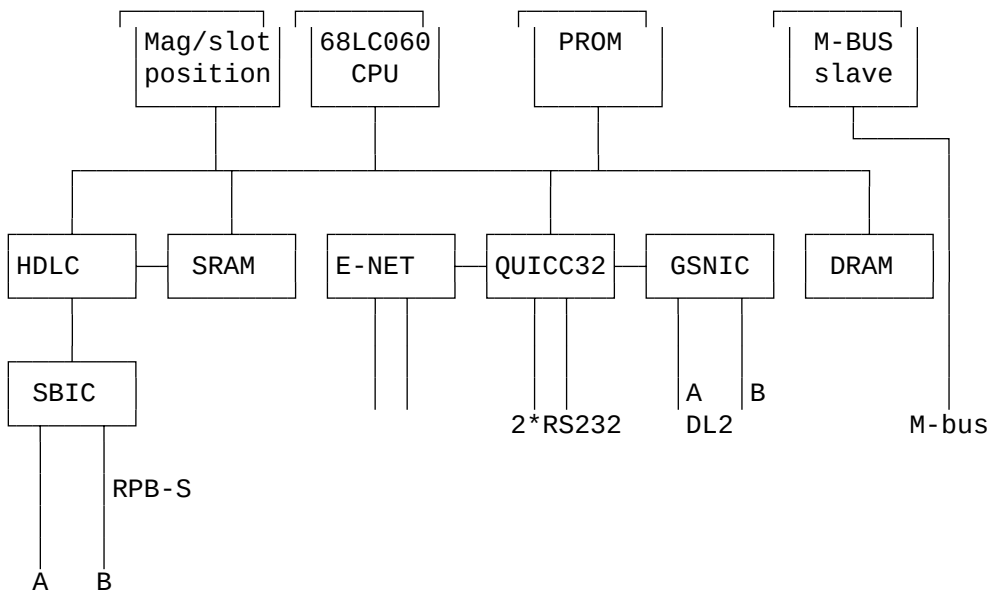


Figure 11. Hardware survey for RPG2

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5.5.2 Functions

Handling of RPB-S.

RPG2 uses a redundant RPB-S/M, path A and B, through the backplane.

When an application signal to an RPG2 occurs SBIC checks the address field in a frame containing an individual RP-address. If the data in the field is equal to RPG2 logical address (previously stored in a register in SBIC) the frame is passed through the circuit to the HDLC controller. The controller strips all except the information field and puts the signal in the in-buffer. The signal is then transferred, by the OS, from the buffer to an application program.

DL2 handling.

DL2B is available in the backplane. A MC68MH360 (QUICC32) works in a companion mode as a communication co-processor for the redundant DL2B connection to the Group Switch. Each of the two DL2B connections has 32 channels of 64 kbit/s.

DL2B is connected to QUICC32 through an ASIC, called GSNIC, which sends 2MB/s HDLC stream to the controller for further processing.

M-bus handling.

RPG2 implements a slave on the M-bus, connected through the backplane.

RPG2 can through the M-bus support the CP with its product individual data, such as product number, revision, name, manufacturing date and serial number. The M-bus also gives the CP access to the MIA indicator on RPG2.

Ethernet.

RPG2 can be connected either to 10Base-T Ethernet (through a 8 pins connector) or to AUI Ethernet (through a 24 pins test and AUI connector), both connectors are available in the front panel.

Supervisory functions.

Hardware supervises parity in the SRAM and DRAM memory. There is also a function for supervising the execution time for programs (watchdog). This function causes an interrupt if the execution time for a program is too long, for example if an infinite loop occurs.

Hardware also contains checks to ensure that addressing outside own program and data area boundaries not can take place.

5.5.3 Physical structure

The RPG2 is designed to fit in a GDM-H magazine together with two RP4s and two DLHB boards. The figure below shows a typically equipped GDM-H magazine seen from the front.

Note that the RPG2 is not limited to this configuration, other magazines can be supported as well.

R	D	R	R	R	R	R	R	R	R	R	D	R
P	L	P	P	P	P	P	P	P	P	P	L	P
4	H	G	G	G	G	G	G	G	G	G	H	4
-	B	2	2	2	2	2	2	2	2	2	B	-
H												H
0	1	2	4	6	8	10	12	14	16	18	19	

Figure 12. GDM-H magazine equipped with RPG2.

- a** Motherboard
- The board contains the following main parts:- DL2B interface implemented in GSNIC.- Doubled Ethernet connection, 10Base-T and AUI Ethernet. Connectors are available in the front panel of the RPG2.- M-bus interface.- Power supply for the board.- RS232 connector which provides 2 channels of RS232 interface.
- b** Daughterboard
- The board contains the following main part- The main processor Motorola 68LC060. - MC68MH360, (QUICC32). - SBIC (Serial Bus Interface Circuit).- HDLC protocol handler.- A dynamic RAM (DRAM) of size 16MByte. - A static RAM (SRAM) of size 128 Kbyte for storage of HDLC circuit microprogram. - An read/Write non volatile memory (FLASH) of size 1MByte.- Reset logic.- Clock logic.

6 Characteristics

6.1 Characteristics for RP2 family

6.1.1 Programming Language for Application Programs

Assembler language ASA21R can be executed in RP2/RP4.

The RP is also designed so that it is compatible with programs written in the assembly language for RP1, ASA210R. (RP1 is described in the subsystem RPS-1.)

Existing ASA210R programs are structured in program pages of 1kW8. This structure can be converted directly to a continuous program code with an upper limit of 64kW16. Existing ASA210R programs can only address a maximum of 4kW8 data.

The ASA210R and ASA21R languages can be mixed in an RP but not in the same program.

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6.1.2 Limits and Properties

The RP2/RP4 has:

16-bit arithmetic

16-bit addressing for both programs and data

maximum program size 64 kW16

maximum data store size/CM 64 kW16

Equipped memory size, 256 KW16 RAM extendable to 512 KW16.

maximum 16 CMs for controlling application programs

maximum 16 CMs for controlling control system programs

maximum 16 application programs

maximum 16 control system programs (not EM-controlling)

maximum 16 EMs

maximum 256 devices per EM.

6.2 Characteristics for RPD family

6.2.1 Programming Language for Application Programs

The programming language for the RPD family is ANSI-C.

6.2.2 Limits and Properties

The RPD member has:

32-bit arithmetic

32-bit addressing for both programs and data.

Maximum program size for one program 2 MW8.

No limitation of data size for one program except the total memory volume.

Equipped memory size, 4 MW8 or 16 MW8 RAM depending on version of PRO20 processor board.

Maximum addressing capacity is 256 MW8.

Maximum 16 CMs for controlling application programs

Maximum 16 CMs for controlling control system programs

Maximum 16 application programs

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Maximum 16 control system programs

The RPG and RPG2 member has:

32-bit arithmetic

32-bit addressing for both programs and data.

Maximum program size for one program 2 MW8.

No limitation of data size for one program except the total memory volume.

Equipped memory size, 16 MW8.

Maximum addressing capacity is 4 GW8.

Maximum 16 CMs for controlling application programs

Maximum 16 CMs for controlling control system programs

Maximum 16 application programs

Maximum 16 control system programs

7

Abbreviations

a AUI

Attachment Unit Interface.

b BIC

Bus Interface Circuit.

c BYB 202

Ericsson's equipment practice.

d BYB 501

Ericsson's equipment practice.

e CM

Control Module.

f CP

Central Processor.

g DL2

Digital Link version 2. 32 64 kbit/s channels. Differential pairs

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h	DL2B DL2 through a backplane.
i	DL3 Digital Link version 3. 256 64 kbit/s channels. Differential pairs
j	DLHB Digital Link Multiplexer Half Height Board. The board fits 16 DL2 frames in one DL3 frame.
k	DS Data Store.
l	EM Extension Module.
m	EMB Extension Module Bus.
n	EMB2 Extension Module Bus version 2.
o	EMBCB-F Extension Module Bus Connection Board Full height.
p	EMBCB-H Extension Module Bus Connection Board Half height.
q	GDM-F Generic Device Magazine Full height.
r	GDM-H Generic Device Magazine Half height.
s	GSNIC Group Switch Interface Circuit.
t	HDLC High level Data Link Control.
u	LED Light Emitting Diode.
v	M-bus

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	Maintenance bus.
w	MIA
	Manual Intervention Acknowledge.
x	OS
	Operating System.
y	PTS
	Program Test System.
z	RDEX
	Regional Executive System of RPD.
aa	RDEXPR
	Boot program of RDEX. Executes in passive mode.
ab	RDEXR
	Executive program of RDEX. Executes in active mode.
ac	REX
	Regional Executive System of RP2.
ad	REXPR
	Boot program of REX. Executes in passive mode.
ae	REXR
	Executive program of REX. Executes in active mode.
af	RGEX
	Regional Executive System of RPG.
ag	RP
	Regional Processor.
ah	RPB
	Regional Processor Bus.
ai	RPB-P
	Regional Processor Bus, Parallel.
aj	RPB-S
	Regional Processor Bus, Serial.
ak	RPB-S/I

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RPB-S, Incoming on cable to and from CP/RPH or preceding RP on the bus branch.

al RPB-S/M

RPB-S, Magazine internal to and from one path in the backplane.

am RPB-S/O

RPB-S, Outgoing on cable to and from next RP on the bus branch.

an RPB-S/X

RPB-S, Crossover cable of both paths to and from twin RP4 in another magazine.

ao RPD

Regional Processor Device.

ap RPG

Regional Processor with Group switch interface.

aq QUICC32

QUad Integrated Communication Controller, 32 channels.

ar RX

Receive direction.

as SBIC

Serial Bus Interface Circuit.

at SNT/DL2

Signalling Network Terminal/Digital Link variant 2.

au TX

Transmit direction.