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SLR/OS/N/ZDT Margareta Persson		2002-12-13	A	

Test Instructions for SCB-RP ROJ 208 323/2

Document History

Describe the document changes below.

Date	From	To	Changes and reason for changes
2002-12-13		A	First released version

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1 Introduction

This document is a test instruction for the system test of the, ROJ 208 323/2 SCB-RP) board (Ref. [1]).

2 Test object

Test is valid for: ROJ 208 323/2

3 Test Sequence

The test is divided into three parts: Initial test, System test and RPB-S test. All three parts are shortly described below.

3.1 Initial Test

This is a test of RAM and it is executed before the SCB-RP starts up. If test passes the SCB-RP boots in a normal way and execution of test programs can start. If test fails Ethernet is initiated from DPRAM and test result can be fetched from board to the test GUI.

3.2 System Test

System test itself is divided into two parts: Maintenance Bus Test and DEST. The tests are shortly described below.

3.2.1 Test of Maintenance bus

This is a test of maintenance bus in GEM (Ref. [2]). The SCB-RP provides the maintenance bus interface. This is implemented as a normal I²C bus. The SCB-RP acts as the master on this bus, but has also a slave interface like all other boards in the GEM magazine. The maintenance bus also gives the possibility to point out specific PBA in a magazine by controlling the MIA-LED. The test of maintenance bus is to turn the MIA-LED on and off within all PBA:s in GEM. The test runs from test GTM (General Test Manager).

3.2.2 DEST

DEST (Downloadable Ethernet based Self-Test) is used for memory tests, FIA processor interface test and read/write operation to certain components connected to processor or FIA. DEST on SCB-RP is divided into 17 subtest. Subtest 1-6 is general for all PBA's using the RPI-block and 11 subtest specific for the SCB-RP. Each of them performs test of some functionality on the PBA or does some necessary set ups used by other subtest. All subtests are briefly described in table 1.

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Table 1: Subtest in DEST for SCB-RP

Subtest	Name of the subtest	Description
	Test of RPI-block	
1	FIA	Test of FIA ASIC, Ctrl logic, addr & data bus
2	Short RAM test	Test of RAM
3	Long RAM test	Test of RAM
4	Temp sensor	Test of temperature sensor in RPI-Block
5	ReadPos	Read out board position and subrack ID
6	Set up	Mask TEA and release reset for applications in FIA
	Test of SCB-RP	
7	Power	Power supervision
8	Interrupt test	Test of interrupt between FIA and CPU
9	Temperature	Reads out actual temperature on Motherboard
10	Temp sensor DB	Test of temperature sensor on Daughter board
11	Glink test	Test of GT-48330, G.Link-to-CPU interface
12	Switch test	Test of switch
13	Switch dump register dev 0	Dump of all registers in GT48360(DD24)
14	Switch dump register dev 1	Dump of all registers in GT48350(DD1)
15	Switch dump register dev 2	Dump of all registers in GT48350(DD5)
16	Switch dump register dev 3	Dump of all registers in GT48350(DD9)
17	Switch dump register dev 4	Dump of all registers in GT48350(DD13)

The DEST downloads and executes from the GTM. If an error appears the DEST generates an error message that reports what part of the test failed, and some more error information

3.3 RPB-S Test

For communication with the CP, the SCB-RP provides an RPB-S interface. RPB-S is connected to the SCB-RP via a front connector and distributed to the backplane. Each RPI in the magazine is connected to two RPB-S/M branches, since there are two SCB-RP boards in each GEM magazine. RP commands are simulated with Serpent. The test is performed by deblocking the RP in SCB-RP board and by sending echo signals to it. RP is then blocked again. PBOOT has to be loaded on the SCB-RP in order to perform this test.

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4 Requirements

4.1 Required material

Qty	Article	Name
1	BFD 508 002/1	GEM
2	ROJ 208 323/2	SCB-RP (test objects)
2	ROJ 208 xxx/x	other GEM boards

4.2 Instrument

Qty	Article	Name
1	-	Test PC
1	-	TFTP-server
1	-	Switch
1	-	PC for Serpent

4.3 Software

Qty	Article	Name
1	CXC 105 189	GTM (<i>Test GUI</i>) Reference [3]
1	CXC 105 188	EBOOT on all PBA's in GEM.
1	CXC 106 0046	PBOOT
1	CXC 105 213	SCB_DEST (SCB test program)
1	CXC XX XXX	OS and some parameters (specific for each index of board)

4.4 Cables

Qty	Article	Name
2	-	Network Cable
2	TSR 491 0274	Ethernet straight (for switch)
2	TSR 491225/x	RB-Bus cable
4	TSR 490 0101/1	-48V
For cables see reference [4].		

5 Set ups before test

5.1 Hardware preparation before test

Place two SCB-RP boards in GEM (in slot 0 and 25). Also place two other GEM boards in the magazine, one in slot 7-9 and the other in slot 14-17 (see figure 1). This is for test of both Ethernet and RP-bus communication from SCB-RP via the back plane.

The diagram illustrates a 26-slot server chassis layout. The slots are numbered 0 through 25. Slots 0, 6, 7, 16, 17, 24, and 25 are populated with various components, including network ports, USB ports, and internal drives. Slots 7 and 17 are highlighted in green, indicating they are occupied by the two 2.5" bays. The remaining slots (1-5, 8-15, 18-23) are empty, representing the available space for the 18 3.5" bays.

Connect the SCB-RP boards to power and Serpent. Connect the SCB-RP board from the Switch to one of the Ethernet ports in the front of the SCB-RP board. Both 100BaseT and 1000BaseT needs to be tested (connection from the switch see figure 2).

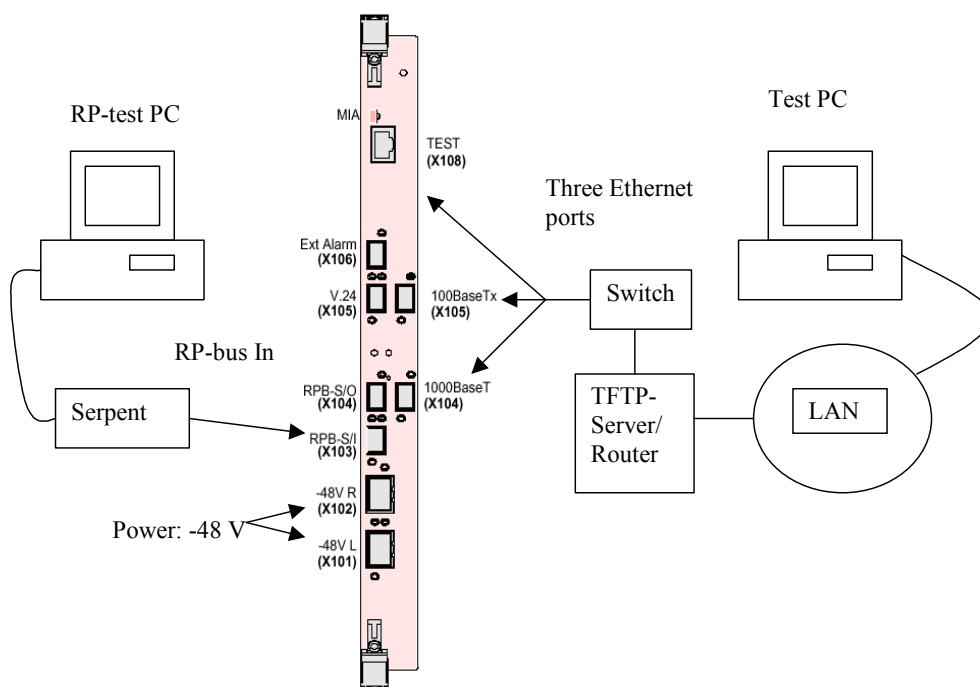


Figure 2. External connections of power and test equipment for SCB-RP.

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5.2 Setting IP-addresses

Ethernet address for a PBA in GEM depends on three things, magazine, slot and left or right SCB-RP. The Ethernet address looks like 192.168.X.YZZ. The first numbers are hard coded in EBOOT, X is the number of the upper address plug in the GEM, Y is 1 if the left SCB should be used and 2 if it is the right SCB and ZZ is the slot number plus 1.

Example: The left SCB-RP in a GEM (slot 0) with number 4 on the upper address plug has the IP-addresses 192.168.4.101 and 192.168.4.201.

6 Test sequence

6.1 Initial Test

After power up, the processor makes a complete RAM test on the board. This RAM test will take some time.

If test passes the board boots in a normal way and execution of system test can start. If test fails Ethernet is initiated from DPRAM.

Test result is then fetched from the board by GTM. See reference [5] for information on fault codes during power up.

6.2 System Test

System test is divided in two parts.

6.2.1 Test of Maintenance bus

This is a test of the maintenance bus in GEM. The test is executed from GTM. The test of the maintenance bus is done by turning the MIA-LED on and off on SCB-RP and to program and verify the ID-prom.

6.2.2 DEST

This is a self-test on the SCB-RP. The test downloads to SCB-RP from GTM. GTM is described in reference [4]. The DEST is placed on the TFTP-server from with the GEM can fetch the program.

The test program number, run by GTM, can be any of the test numbers specified in table 1 page 3. That is test 1-6 for RPI part and test 7-17 specific for SCB.

These tests are also combined into test sequences, numbered 101-103, and runs automatic in GTM. Test flow 101 runs subtest 1-8 (test of mother board). This test flow runs during start up of test. Test flow 102 runs 1-8, 10-12 (test of both mother and daughter board) This test flow runs during heat test. Test flow 103 is for debug of the switch and run subtests 6,10-12. After test check the messages for correct slot and address plug is OK. If there are one or more errors, the test failed. See below what different error codes mean. Otherwise if there is no error, the test has passed.

Note: Because of there can be the same position name on components on the mother- and daughter board, the position is written DXX for the mother board and DDXX for the daughter board.

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6.2.2.1 Subtest details

Subtest 1-6 is for all boards with RPI-core. Subtest 1-9 is for the mother board and subtest 10-17 is for the daughter board.

Subtest 1

Test of interface between CPU and FIA ASIC.

Index 1

Data bus stuck fault and opens test. Write and read 0's and 1's at lowest and highest address.

If there is a fault, the following error code is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 2: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 2

Walking '1' for FIA SRAM (data).

If there is a fault, the following error codes is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 3

Walking '0' for FIA SRAM (data).

If there is a fault, the following error codes is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 4

Address bus stuck faults, opens and shorts test. Walking '1' and '0' for FIA SRAM.

If there is a fault, the following error codes is issued:

Error code 1: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 2: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 3: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 4: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 5: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Error code 6: Read/Write to (FIA D32) internal SRAM failed at address 0xXX.

Index 5

March test of SRAM. Enable the internal FIA SRAM, and define the start address at 0xD0000000.

No test is performed in this subtest.

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Index 6

March test of SRAM. Read background 0x00 and write 0xFF.

If there is a fault, the following error code is issued:

Error code 1: March test on FIA internal SRAM failed at address 0xXX.

Index 7

March test of SRAM. Read background 0xFF and write 0x00.

If there is a fault, the following error code is issued:

Error code 1: March test on FIA internal SRAM failed at address 0xXX.

Index 8

March test of SRAM. Read background 0x00.

If there is a fault, the following error code is issued:

Error code 1: March test on FIA internal SRAM failed at address 0xXX.

Index 9

Checkerboard test of SRAM. Write background 0xAA at even addresses and 0x55 at odd addresses.

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on FIA internal SRAM failed at address 0xXX.

Index 10

Checkerboard test of SRAM. Write background 0x55 at even addresses and 0xAA at odd addresses.

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on FIA internal SRAM failed at address 0xXX.

Index 11

March test of RPBSIC in FIA. Write background 0x00.

No test is performed in this subtest.

Index 12

March test of RPBSIC in FIA. Read background 0x00 and write 0xFF.

If there is a fault, the following error code is issued:

Error code 1: March test on RPBSIC in FIA failed at address 0xXX.

Index 13

March test of RPBSIC in FIA. Read background 0xFF and write 0x00.

If there is a fault, the following error code is issued:

Error code 1: March test on RPBSIC in FIA failed at address 0xXX.

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Index 14

March test of RPBSIC in FIA. Read background 0x00:

If there is a fault, the following error code is issued:

Error code 1: March test on RPBSIC in FIA failed at address 0xXX.

Index 15

Checkerboard test of RPBSIC in FIA. Write background 0xAA at even addresses and 0x55 at odd addresses

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on RPBSIC in FIA failed at address 0xXX.

Index 16

Checkerboard test of RPBSIC in FIA. Write background 0x55 at even addresses and 0xAA at odd addresses

If there is a fault, the following error code is issued:

Error code 1: Checkerboard test on RPBSIC in FIA failed at address 0xXX.

Subtest 2

Short memory test.

Tests the data bus and the address bus.

It is divided into 5 indexes, all of them described below.

Index 1

Data bus stuck fault and opens test. Writing 0's to the lowest address and 1's to the highest, and then reading the values back do this.

If there is a fault, the following error codes is issued:

Error code 1: Cannot write to lowest address in DRAM.

Error code 2: Cannot write to highest address in DRAM.

The values read back is printed out along with what was expected.

Index 2

This test checks if the data bus (32 bits) to DRAM is OK.

The test is performed using walking 0 and walking 1 tests, this means that one bit on the data bus is set to 0 or 1 and all the other bits is set to the opposite value.

The walking 1 data is sent to the lowest address in DRAM and the walking 0 data is sent to the highest address in DRAM. The data is then read back to verify that the bit value has not changed. The bit is then shifted one step and then the write, read and verify is done all over again, this continue until all bits have been tested.

If there is a fault, the following error codes is issued:

Error code 1: Error when rotating 1 on data-bus. Faulty bits 0XXXXXXXXX

Error code 2: Error when rotating 0 on data-bus. Faulty bits 0XXXXXXXXX

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Faulty data bus bits are reported in “Error detail”, in hex format 0XXXXXXXX, where the X’s represents faulty bits during the test.

E.g. 0x00000003 indicates that the two lowest data bits is faulty.

The information in “Error detail” is also printed in the text message.

Index 3

Address bus stuck fault and opens test. Writing 0xFF to the lowest byte and 0x00 to the highest, and then reading the values back do this.

If there is a fault, the following error codes is issued:

Error code 1: Error when writing to ram base. (Address 0x00000000)

Error code 2: Error when writing to ram top. (Address 0xFFFFFFFF)

The values read back is printed out along with what was expected.

Index 4

DRAM address bus test using walking 1. (32 bits)

This means that the first bit on the address bus is set to ‘1’ and all the other bits is set to ‘0’. Then the test data (0x00) is written to that address and read back to verify that the data has not changed. The data is also compared with the content in ram base. The bit is then shifted one step and then the write, read and verify is done all over again, this continue until all bits have been tested.

If there is a fault, the following error codes is issued:

Error code 1: Error in ram base when rotating 1 on address bus.

Error code 2: Error when rotating 1 at current address.

Error code 3: Error, bits stuck to '0' when rotating 1 on address bus.

Faulty data is reported in ‘Error detail’ and in ‘address’, ‘expected’ and ‘received’. For error code 1 Error detail show the current address tested. ‘Address’, ‘expected’ and ‘received’ show the content of ram base.

For error code 2 Error detail is not used. ‘Address’, ‘expected’ and ‘received’ show the content of the address tested.

For error code 3 faulty address bus bits are reported in “Error detail”, in hex format 0XXXXXXXX, where the X’s represents faulty bits during the test.

E.g. 0x00000003 indicates that the two lowest address bits is faulty.

The information in “Error detail” is also printed in the text message. ‘Address’, ‘expected’ and ‘received’ is not used.

Index 5

DRAM address bus test using walking 0. (32 bits)

This means that the first bit on the address bus is set to ‘0’ and all the other bits is set to ‘1’. Then the test data (0xFF) is written to that address and read back to verify that the data has not changed. The data is also compared with the content in ram top. The bit is then shifted one step and then the write, read and verify is done all over again, this continue until all bits have been tested.

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If there is a fault, the following error codes is issued:

Error code 1: Error in ram top when rotating 0 on address bus.

Error code 2: Error when rotating 0 at current address.

Error code 3: Error, bits stuck to '1' when rotating 0 on address bus.

Faulty data is reported in 'Error detail' and in 'address', 'expected' and 'received'.

For error code 1 Error detail show the current address tested. 'Address', 'expected' and 'received' show the content of ram base.

For error code 2 Error detail is not used. 'Address', 'expected' and 'received' show the content of the address tested.

For error code 3 faulty address bus bits are reported in "Error detail", in hex format 0XXXXXXXXX, where the X's represents faulty bits during the test.

E.g. 0xC0000000 indicates that the two highest data bits is faulty.

The information in "Error detail" is also printed in the text message. 'Address', 'expected' and 'received' is not used.

Subtest 3

Long memory test.

Tests the DRAM circuits.

It is divided into 2 indexes, both of them described below.

For all of the test steps in subtest 3 there is a limit to the number of errors that will be printed out.

Index 1

March test of all address locations. This test is divided into 4 test steps.

1. Write value 0x00000000 at incremented address.
2. Read back value 0x00000000 and write 0xFFFFFFFF at incremented address.
3. Read back value 0xFFFFFFFF and write 0x00000000 at decremented address.
4. Read back value 0x00000000 at incremented address.

If there is a fault, the following error codes is issued:

Error code 1: Error when reading current address. (Test step 2)

Error code 2: Error when reading current address. (Test step 3)

Error code 3: Error when reading current address. (Test step 4)

The address where the fault occurred and the values read back is printed out along with what was expected.

Index 2

Checkerboard test of all address locations. This test is divided into 2 test steps.

1. Write 0xAAAAAAAA to all even addresses and 0x55555555 to all odd addresses, then read back and verify all values.
2. Write 0x55555555 to all even addresses and 0xAAAAAAAA to all odd addresses, then read back and verify all values.

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If there is a fault, the following error codes is issued:

Error code 1: Error when reading current address. (Test step 1)

Error code 2: Error when reading current address. (Test step 2)

The address where the fault occurred and the values read back is printed out along with what was expected.

Subtest 4

Test of temperature sensor LM75 (D31).

The test is divided into five parts described below.

Index 1

Read out content of the Tos and the Thyst registers and compare them with the default reset values. Default value of the Tos register is 80 degrees Celsius and of the Thyst register is 75 degrees Celsius. The temperature sensor is connected to the CPU via an I2C-interface.

If there is a fault, the following error codes is issued:

Error code 1 Tos register does not contain the programmed value of 80 degrees Celsius in D31!

Error code 2: Thyst register does not contain the programmed value of 75 degrees Celsius in D31!

Index 2

Write 100 degrees Celsius to the Tos register and 90 degrees Celsius to the Thyst register.

No test is performed in this index.

Index 3

Read out content of the Tos and the Thyst registers and compare them with the "should-be-values" which were set in the Index 2, i.e. 100 degrees Celsius for Tos and 90 degrees Celsius for Thyst.

If there is a fault, the following error codes is issued:

Error code 1 Tos register does not contain default value of 100 degrees C in D31!

Error code 2: Thyst register does not contain default value of 90 degrees C in D31!

Index 4

Write 80 degrees Celsius to the Tos register and 75 degrees Celsius to the Thyst register. These are the default values (see Index 1) and should be restored.

No test is performed in this index.

Index 5

Read out content of the Tos and the Thyst registers and compare them with the values written in Index 4.

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If there is a fault, the following error codes is issued:

Error code 1: Tos register does not contain the programmed value of 80 degrees Celsius in D31!

Error code 2: Thyst register does not contain the programmed value of 75 degrees Celsius in D31!

Subtest 5

Read out board position and subrack ID

Index 1

This test reports four messages to GTM with information of what value the tree address plugs and board position in the GEM magazine. Check that these values are correct.

If there is a fault, the following error codes is issued:

Error code 1: Parity error for AP0 check address plug in upper position in GEM

Error code 2: Parity error for AP1, check address plug in middle position in GEM!

Error code 3: Parity error for AP2, check address plug in lower position in GEM!

Subtest 6

Set up for applications connected to the RPI-core.

Index 1

Settings in CPU or FIA for components connected to the RPI-core

No test is performed in this subtest.

Subtest 7

Test of the power supervision. Check if there is -48 V on the Front connectors on SCB

Index 1

Test of power on the right side of the magazine.

If there is a fault, the following error codes is issued:

Error code 1: Missing -48V on right side of the magazine from the right SCB-RP!

Error code 2: Missing -48V on left side of the magazine from the right SCB-RP!

Error code 3: Missing -48V on right SCB in the magazine!

Index 2

Test of power on the left side of the magazine.

If there is a fault, the following error codes is issued:

Error code 1: Missing -48V on right side of the magazine from the left SCB-RP!

Error code 2: Missing -48V on left side of the magazine from the left SCB-RP!

Error code 3: Missing -48V on left SCB in the magazine!

Subtest 8

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Test of interrupt between FIA and MPC860.

Index 1

Mask all interrupts in MPC860 and FIA.

If there is a fault, the following error codes is issued:

Error code 1 Interrupts not disabled in CPU (D29)!

Error code 2: Interrupts not disabled in FIA (D32)!

Index 2

Release reset for dl-link in FIA_APPZ_RSTR register. Because of there are no dl2_link connected to the SCB-board an interrupt, DL2IRQ, will be set in FIA_RSR. Check if there are any interrupts active by reading the RSR register in FIA.

If there is a fault, the following error codes is issued:

Error code 1 There are interrupts in FIA (D32), should be cleared!

Error code 2: There are not any interrupts in FIA (D32), should be present!

Index 3

Enable all the interrupts from FIA and check MPC860 for pending interrupt from FIA.

If there is a fault, the following error codes is issued:

Error code 1 Interrupts not enabled in FIA (D32)!

Error code 2: Interrupt between FIA (D32) and CPU (D29) does not work!

Index 4

Mask all interrupt and reset for dl-link in FIA and clear FIA-RSR.

If there is a fault, the following error codes is issued:

Error code 1 There is interrupts in FIA (D32), should be cleared

Subtest 9

Temperature on the mother board.

Index 1

Read out the actual temperature from the temperature sensor LM75 (D31) on the motherboard. This subtest returns a message to the GTM with the temperature.

No test is performed in this subtest.

Subtest 10

Test of temperature sensor LM75 (DD27) on the daughter board.

Same test is performed as subtest 4.

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Subtest 11

Test of the GT48330 (DD17), G.link-to-CPU interface. This test is also a test of the interface between mother and daughter board.

Index 1

Read from G.link control 1 register, initial value 0x16.

If there is a fault, the following error codes is issued:
Error code 1: Error when read from GT48330 (DD17).

Index 2

Checkerboard and March test on data bus.

If there is a fault, the following error codes is issued:
Error code 1: Stuck-at fault at data or address bus on GT48330 (DD17)!
Error code 2: Stuck-at fault at data or address bus on GT48330 (DD17)!
Error code 3: Stuck-at fault at data or address bus on GT48330 (DD17)!
Error code 4: Stuck-at fault at data or address bus on GT48330 (DD17)!

Index 3

Rotating '1' and '0' on data bus.

If there is a fault, the following error codes is issued:
Error code 1: Data bus error on GT48330 (DD17) at bit 0xXX (walking '1')!
Error code 2: Data bus error on GT48330 (DD17) at bit 0xXX (walking '0')!

Index 4

Check for interrupt in FIA. Some time an interrupt accurse when there is an error in component or in the interface. This error generates an interrupt in FIA. This index is a check for that.

If there is a fault, the following error codes is issued:
Error code 1: There are interrupts in FIA (D32)!

Note: If an error accurse in this subtest there is a possibility suspect that the error is in the interface between the mother and daughter board in the Nexlev plug (X1, DX5).

Subtest 12

Test of the GT48303, GT48360, the four GT48350 and the PHY:s connected to this components.

Index 1

Install devices in Switch for enabling test. This index makes some set-ups. No test is performed in this index.

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Index 2

Initialise the switch devices. Perform a first test of the switch during to read out the contain of DEVICE_TYPE register in GT48350 and GT48360 components

If there is a fault, the following error codes is issued:

Error code 1: Unable to read from DEVICE_TYPE register dev: X!

Error code 2: Fails when reading from DEVICE_TYPE register dev: 0 (DD24)!

Error code 3: Fails when reading from DEVICE_TYPE register dev: X!

Note: Device X is following component.

Dev: 0 = DD24

Dev: 1 = DD1

Dev: 2 = DD5

Dev: 3 = DD9

Dev: 4 = DD13

Index 3

Tests of receive and transmit bus between the different GALILEO components on SCB-RP

If there is a fault, the following error codes is issued:

Error code 1: Unable to read from INTERRUPT_MASK register dev: X!

Error code 2: Fails when read from INTERRUPT_MASK register dev: X !

Error code 3: Unable to read from INTERRUPT_MASK register dev: X!

Error code 4: Fails when read from INTERRUPT_MASK register dev: X !

Error code 5: Unable to read from INTERRUPT_MASK register dev: X!

Error code 6: Fails when read from INTERRUPT_MASK register dev: X !

Error code 7: Unable to read from INTERRUPT_MASK register dev: X!

Error code 8: Fails when read from INTERRUPT_MASK register dev: X !

Index 4

Read out PHY Identifier Register in BCM5401 and LTX9784 on SCB-RP

If there is a fault, the following error codes is issued:

Error code 1: Fails when read from BCM5401(DD22) ID register 1!

Error code 2: Fails when read from BCM5401(DD22) ID register 2!

Error code 3: Fails when read from LXT9784 ID register 1, PHY : X!

Error code 4: Fails when read from LXT9784 ID register 2, PHY : X!

Note: PHY X is following component.

PHY: 0 = DD22

PHY: 1 = DD4

PHY: 2 = DD8

PHY: 3 = DD12

PHY: 4 = DD16

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Subtest 13

Switch dump register device 0: GT48360 (DD24).

Index 1

Register dump of all registers in GT48360 (DD24) on SCB-RP. This subtest returns a lot of messages to the GTM with register name and value.

No test is performed in this subtest.

Subtest 14

Switch dump register device 1: GT48350 (DD1).

Index 1

Register dump of all registers in GT48350 (DD1) on SCB-RP. This subtest returns a lot of messages to the GTM with register name and value.

No test is performed in this subtest.

Subtest 15

Switch dump register device 2: GT48350 (DD5).

Index 1

Register dump of all registers in GT48350 (DD5) on SCB-RP. This subtest returns a lot of messages to the GTM with register name and value.

No test is performed in this subtest.

Subtest 16

Switch dump register device 3: GT48350 (DD9).

Index 1

Register dump of all registers in GT48350 (DD9) on SCB-RP. This subtest returns a lot of messages to the GTM with register name and value.

No test is performed in this subtest.

Subtest 17

Switch dump register device 4: GT48350 (DD13).

Index 1

Register dump of all registers in GT48350 (DD13) on SCB-RP. This subtest returns a lot of messages to the GTM with register name and value.

No test is performed in this subtest.

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6.2.3 Requirements after System Test

The SCB-RP board have to be restarted to get rid of the DEST program. Software like OS, parameters and PBOOT is then to be downloaded to SCB-RP. These files are placed on the TFTP-server. Then the SCB-RP is restarted again as the last part in System Test. All this is done automatically in GTM.

6.3 RP Test

This is a test of RP on PBA. The test is performed from GTM via RP-Test PC connected to Serpent. This test should deblock and block the RP on the PBA. The test passes if RP goes up in working and down to block again. This test is described in reference [4].

7 Faulty boards

If a board don't pass a test, the board serial number, test number, index number, error code and other error data from the fault is written to a log file.

8 Requirements after test

If all tests pass put a label with "SYS OK" on the PBA

9 Abbreviation

CPU	Central Processor Unit
DEST	Downloadable Ethernet based Self Test
DPRAM	Dual-Port Random Access Memory
EBOOT	Ethernet BOOT
FIA	Support ASIC for the MPC860 processor
GEM	Generic Ericsson Magazine
GTM	GEM Test Manager
GUI	Graphic User Interface
I ² C	Inter-Integrated Circuit
PBA	Printed Board Assemble
RP	Regional Processor
RPB	Regional Processor Bus
RPB-S	Serial RP Bus
SCB	Support and Control Board
SDRAM	Synchronous Dynamical Random Access Memory

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10 References

Ref.	Document name	Document number
1	DS SCB_RP	10262-ROJ 208 323/1
2	DS for GEM	102 62-BFD 508 002/1
3	GTM	1551-CNZ 105 189
4	Cables in GEM	1/0363-3/FCP 105 1003
5	EBOOT	1551-CXC 105 188