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Design Specification
Gigabit Ethernet Switch Board
GESB

Abstract: This document contains the design specification of the GESB.

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1 GENERAL

1.1 BACKGROUND

The APZ303 platform will utilise GEM magazines and SCB-RP boards together with processor boards and when applicable, *an Ethernet switch to connect different magazines* running Solaris and Ronja/DPE middle-ware.
The APZ302 platform will utilise GEM magazines and SCB-RP boards together with processor boards and switch running TelORB.
This *Design Specification,* describes a new board: a ***Gigabit Ethernet Switch Board (GESB)***, used to interconnect all the sub-racks in a node.

1.2 PURPOSE

The purpose of this document is to define the base conditions required for the physical design of the GESB.
The RPI part of the GESB is only covered briefly, since it is described in detail in the design specification RPIHW1A, see reference 4.

1.3 INTRODUCTION

The GESB is going to be used in the GEM. For redundancy reasons the two GESB will be placed in two different GEM sub rack.
The GESB serves a number of main functions:

- GESB is an 8-port Gigabit Ethernet switch, able to handle communication between boards in GEM as well as communication to GEM-external stations.
- GESB houses an RPI.

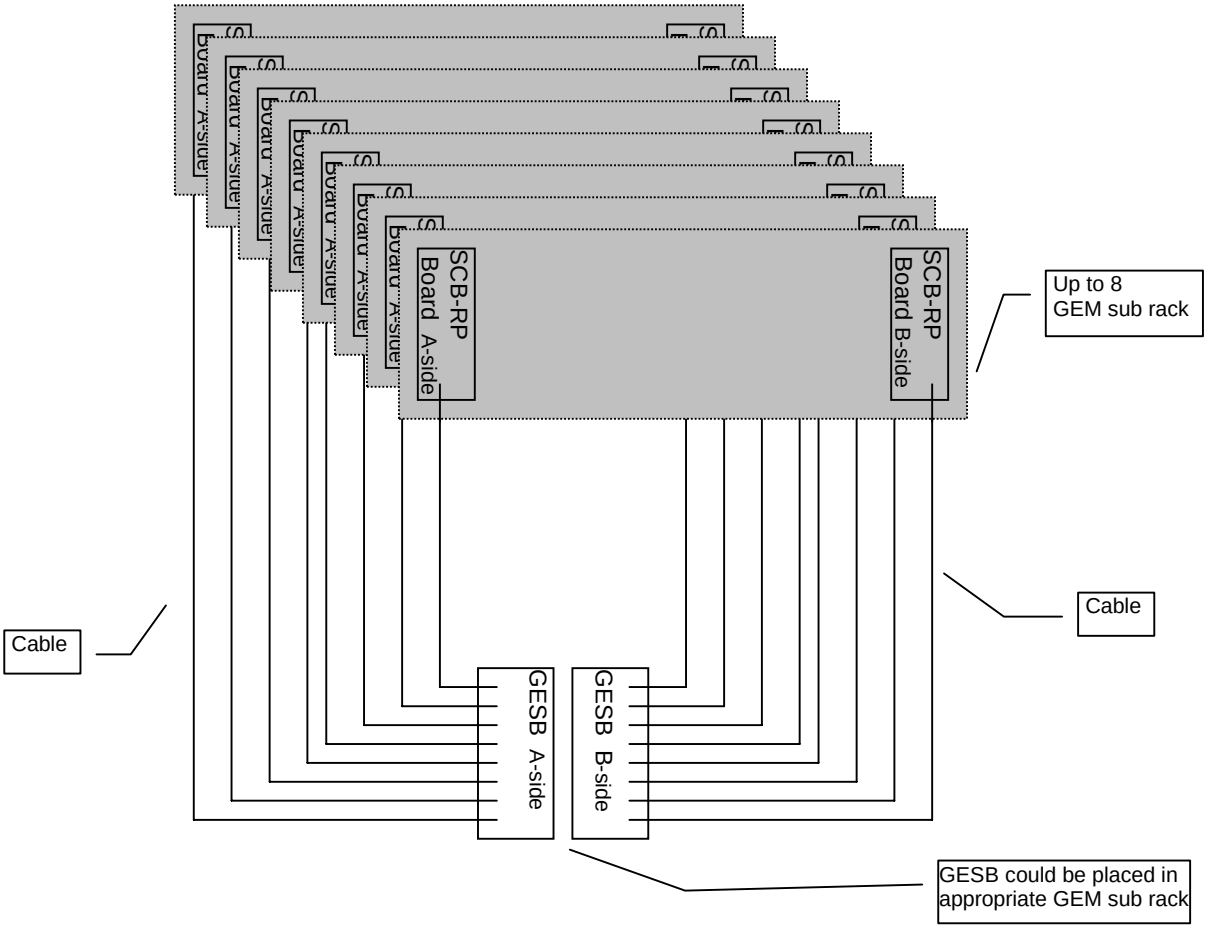

Figure 1: Schematic overview of the GESB

1.4 DEFINITIONS

The words *MPC860P*, *CPU*, and *MPC* are used synonymously and have always the same meaning throughout this document.

1.5 REVISION HISTORY

Revision	Date	Prepared	Major changes
PA1	01-01-06	Jan Wrang	First draft
PA2	01-01-15	Jan Wrang	Second draft. Comments from review meeting 2001-01-09.
PA3	01-01-22	Jan Wrang	Third draft. Comments from review meeting 2001-01-18.
PA4	01-01-30	Jan Wrang	Fourth draft.
A	01-02-12	Jan Wrang	Approved at review meeting 2001-02-07.
B	01-04-11	Jan Wrang	Smaller PHY circuit. Front-connector numbering. External QBus arbiter. Test interface.
C	01-08-20	Jan Wrang	Removed unmanaged I^2C mode, changed port numbering.

2 FUNCTIONAL DESCRIPTION

The three main parts of the GESB are the *Gigabit Ethernet switch,* the *RPIHW1A_GESB module* (management CPU) and the *additional parts*. A block diagram of the GESB is shown below:

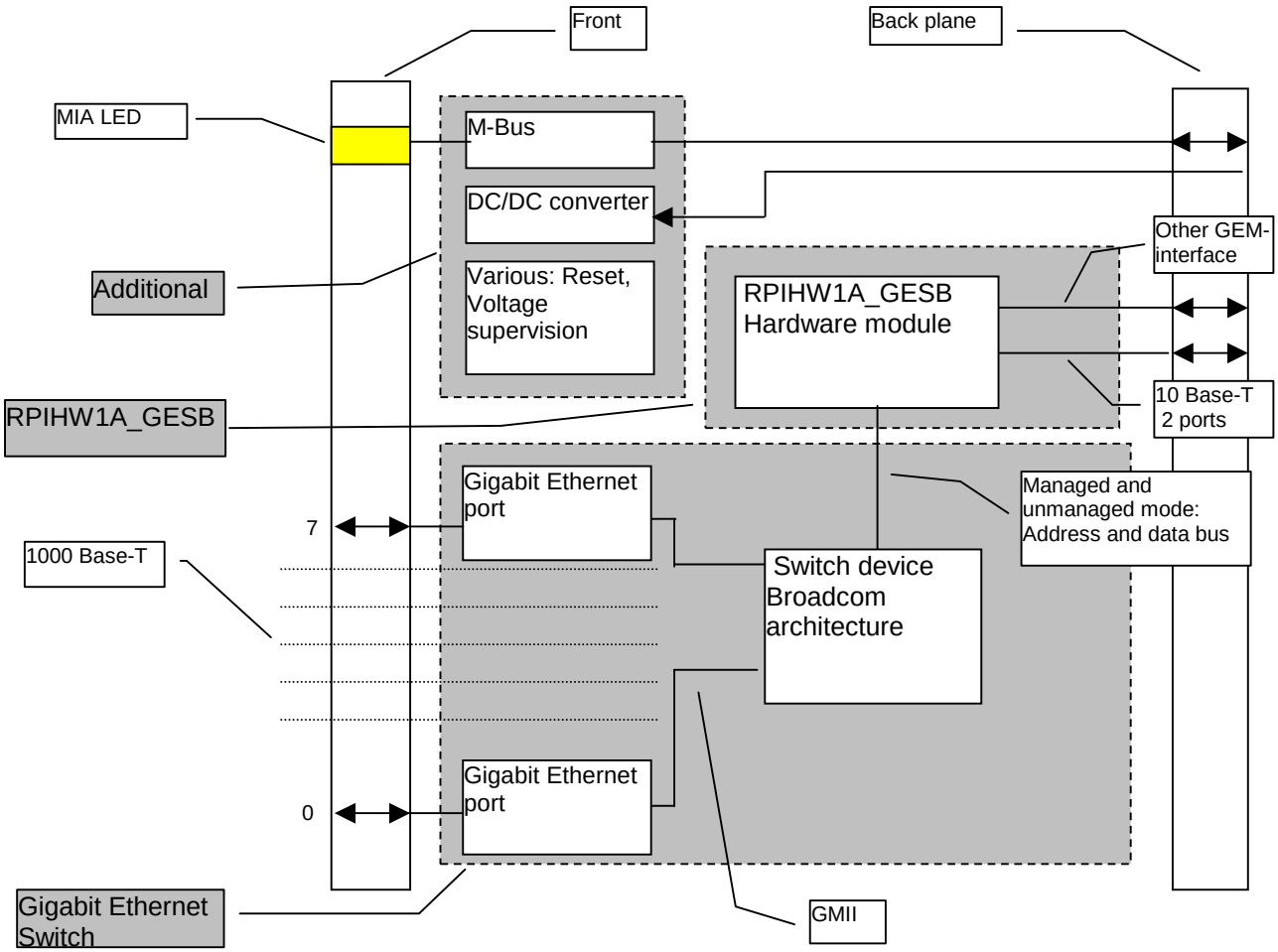

Figure 2: Block diagram of the GESB

2.1 OVERVIEW

For the 8 Gigabit ports one board is enough (but the width must be 30 mm due the power dissipation).

2.1.1 Gigabit Ethernet switch.

The main features of the Gigabit Ethernet switch are the following:

- Provides eight 1000Base-T ports towards the front.
- All front connectors are the 8 pin RPV 431 1911 (20 mm pitch).
- All Ethernet ports support auto-negotiation.
- All Ethernet ports support half or full duplex communication.
- The switch provides automatic MAC address learning.
- The Ethernet switch support operation in managed and unmanaged mode.
- Flow control complies with IEEE 803.x can be enabled.
- The switch can be configured for VLAN support
- PCI bridge to the management CPU

2.1.2 RPIHW1A_GESB module.

The RPIHW1A exist as a symbol in Concept (see reference 9).
There is however a need to connect directly to the MPC860P address/data bus for the PCI bridge. That means that some design work has to be done inside the RPIHW1A symbol and a new symbol name RPIHW1A_GESB is needed.
The main features of the RPIHW1A_GESB are the following:

- Equal interfaces as other boards in the GEM.
- Equal software as other boards in the GEM.
- Reset, temperature supervision,
- Interface to QSpan II circuit.

The RPIHW1A_GESB block is described very briefly in this design specification. It is handled as a symbol with interface to the back plane and surrounding hardware. For more information see reference 4.

2.1.3 Additional parts

Additional parts are:

- Maintenance bus-interface (M-bus); GEM concept.
- Reset (power on, hard and soft); GEM concept.
- Voltage supervision.
- DC/DC converters.

2.2 GIGABIT ETHERNET SWITCH

The Ethernet switch is build of a chipset from Broadcom Corporation.
The chip BCM5680 offers eight ports of 10, 100 or 1000 Mbit/s connectivity with on-chip packet buffering.

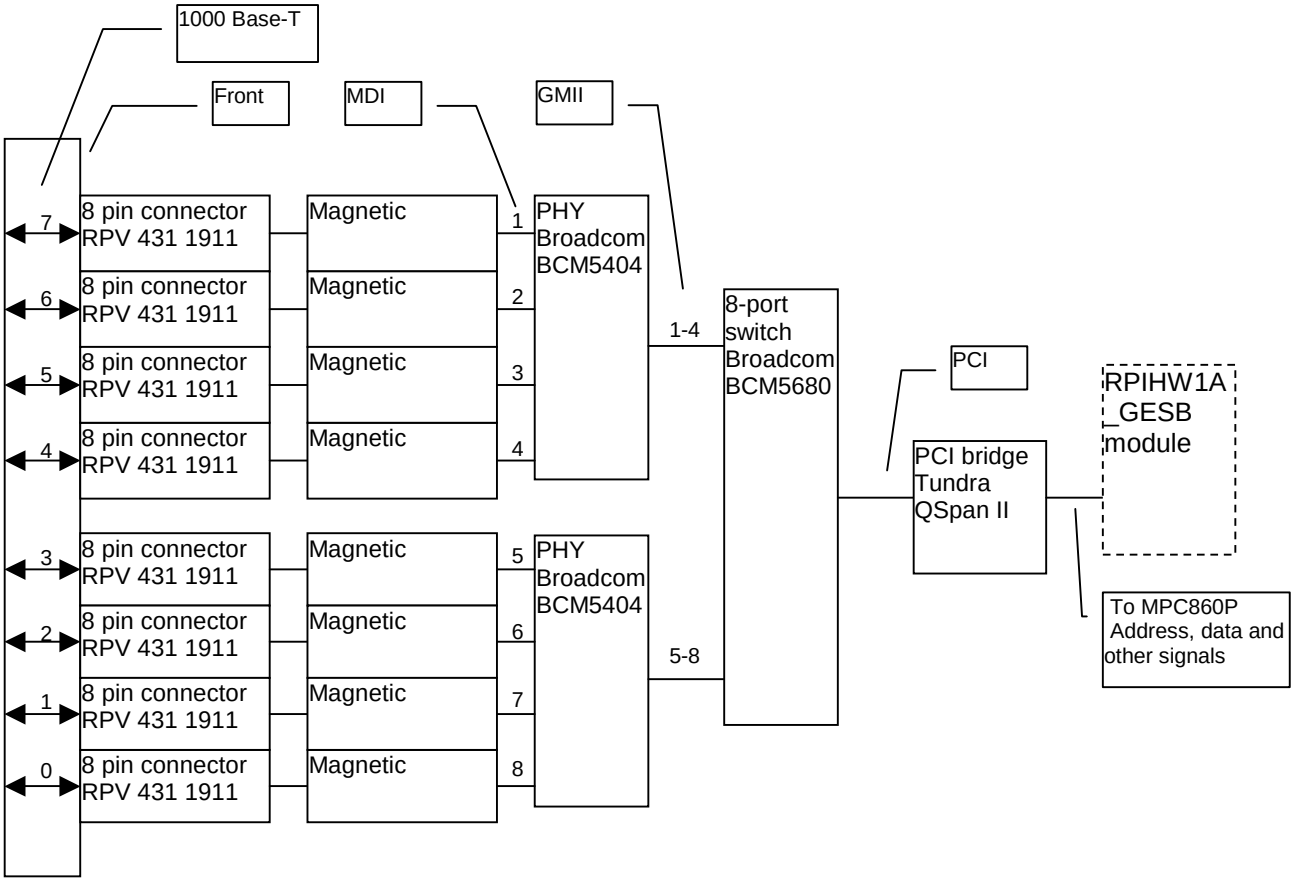

Figure 3: Block diagram of the Gigabit Ethernet Switch

For the unmanaged and the managed mode, the BCM5680 provides a PCI bus interface. However a PCI bridge is needed (the QSpan II from Tundra), to interface to the MPC860P.
The chip BCM5404 (from Broadcom) consists of four triple speed Gigabit Ethernet transceiver.
The magnetic contains four 1:1 isolation transformers with built-in common mode chokes.
Note the numbering of the ports: The front port 7 (at the top) corresponds to port 1 for the BCM5404 and the BCM5680. In a similar way the front port 0 (at the bottom) corresponds to port 8 for the BCM5404 and the BCM5680.

2.2.1 8-port Gigabit switch, BCM5680

BCM5680:

- Implements two mechanisms to prevent Head Of Line (HOL) Blocking on a per-port basis: cell-based HOL blocking and packet-based HOL blocking. (A mechanism, which prevents packets from being sent to a “blocking” port. A port may become blocking when “too many” packets are queued to this port. The concept adopts the approach that it is preferable to discard packets to congested ports than to allow them to consume more and more buffers, as eventually other ports will become blocked too, due to a shared buffer pool).
- Integrated 512kB data packet memory.
- Integrated 8k MAC address table with auto learning.
- Supports a packet ageing mechanisms, which allows the BCM5680 to discard a packet residing in the switch packet memory. The packet ages limit, are programmable and have a maximum duration of approximately 1-second.
- Supports mechanisms to handle backpressure allowing for flexible flow control on packet transactions. The limit at which backpressure is detected is based on the amount of memory utilised by the packets on an input port. The limit is programmable on a per-port basis. (Backpressure is the processes of controlling data transmission at the sender to avoid overfilling receive buffers and loss of data at the receiver).
- Provides programmable threshold limits to prevent packets from flooding into other parts of the network.
- Supports up to four Class of Services (CoS) queues per egress port.
- Support port mirroring of any port.
- Fully compliant with the IEEE 802.1D spanning-tree support specifications.
- Supports the IEEE 802.1p specification for traffic class expediting and dynamic multicast filtering support (Class of Service, or CoS).
- Supports the IEEE 802.1Q specification for virtual Bridged Local Area Networks.
- Provides mechanism by which up to eight ports of the same speed can be bundled together to form a port bundle or trunk group. Up to six trunk groups can be established. (Port trunking provides for increased bandwidth between two Ethernet stations by allowing multiple “physical” links to be combined to operate as a single “logical” link).
- Supports inclusive filtering to enable a switch application to filter and classify packets based on certain protocol fields in the packet. Filters can be used defined fields from layer 2 to Layer 7 within a frame.

Due to the heat dissipation (max 8-9W), a heat sink is required for the BCM5680. See also reference 20

2.2.2 Quad PHY, BCM5404

The BCM5404 incorporates four PHY into one single chip device that performs all the physical layer interface functions for 1000Base-T and 100BaseTx, and 10BaseT Ethernet on CAT 5 UTP cable.
The device performs:

- Encoding (In 1000BASE-T mode, the BCM5404 simultaneously transmits and receives a continuous data stream on all four twisted pairs in the CAT 5 cable. Byte wide data from the transmit data pins is scrambled, trellis encoded into a 4-dimensional code group (a PAM5 symbol on each of the four twisted pairs), and inserted into the transmit data stream.)
- Decoding (In 1000BASE-T mode, the received data stream passed through the Viterbi decoder, de-scrambled, and translated back into byte wide data.)
- Data recovery and clock recovery (The clock recovery and generator block creates the 125 MHz transmit and receive clocks.).
- Stream cipher (In 1000BASE-T mode, the GMII transmit data is scrambled by exclusive-OR'ing the input data byte with an 8-bit wide cipher text word.)
- Digital adaptive equalisation (The digital adaptive equaliser removes inter-symbol interference by the transmission channel media.)
- Echo cancellation (Because of the bi-directional nature of the channel in 1000BASE-T, an echo impairment is caused by each transmitter. The echo canceller removes the transmitted signal impairment from the incoming receive signals.)
- Management functions (The status and Control Registers of the BCM5404 are accessible through the MDIO and MDC serial interface.)

The BCM5404:

- Is fully compliant with the IEEE 802.3 standard.
- Supports auto-negotiation between all three speeds. It also features an automatic MDI crossover function, thus eliminates the need of crossover cables.
- During 1000Base-T operation, the BCM5404 has the ability to automatically detect and correct some cable wiring errors. (This includes polarity errors caused by swapping of wires in a pair as well as swapped pairs.)

Due to the heat dissipation (max 5W), a heat sink is required for the BCM5404. See also reference 20.

2.2.3 Magnetic

The implementation of triple speed operation requires the use of simple magnetic containing four 1:1 isolation transformers with built-in common mode chokes.
Bel Fuse has two different packages: 17,53 mm width (16,38 mm length) or 13,26 mm width (20,57 mm length).
To fit with the connector width (20.0 mm pitch) the width of 17.53 mm and 13,26 mm is possible.

S558-5999-P3 (17,53 mm width) was used on the SCB-RP board. Therefore the chosen magnetic is S558-5999-P3 from Bel Fuse.

2.2.4 Ethernet Management Support

Via the Ethernet Management interface the CPU have read/write access to the Ethernet switch. This allows following functions to be supported:

- (Re-)Configuration of the Ethernet switch
- Collecting of network statistics
- VLAN support
- Port monitoring (sniffer function)
- Spanning tree support

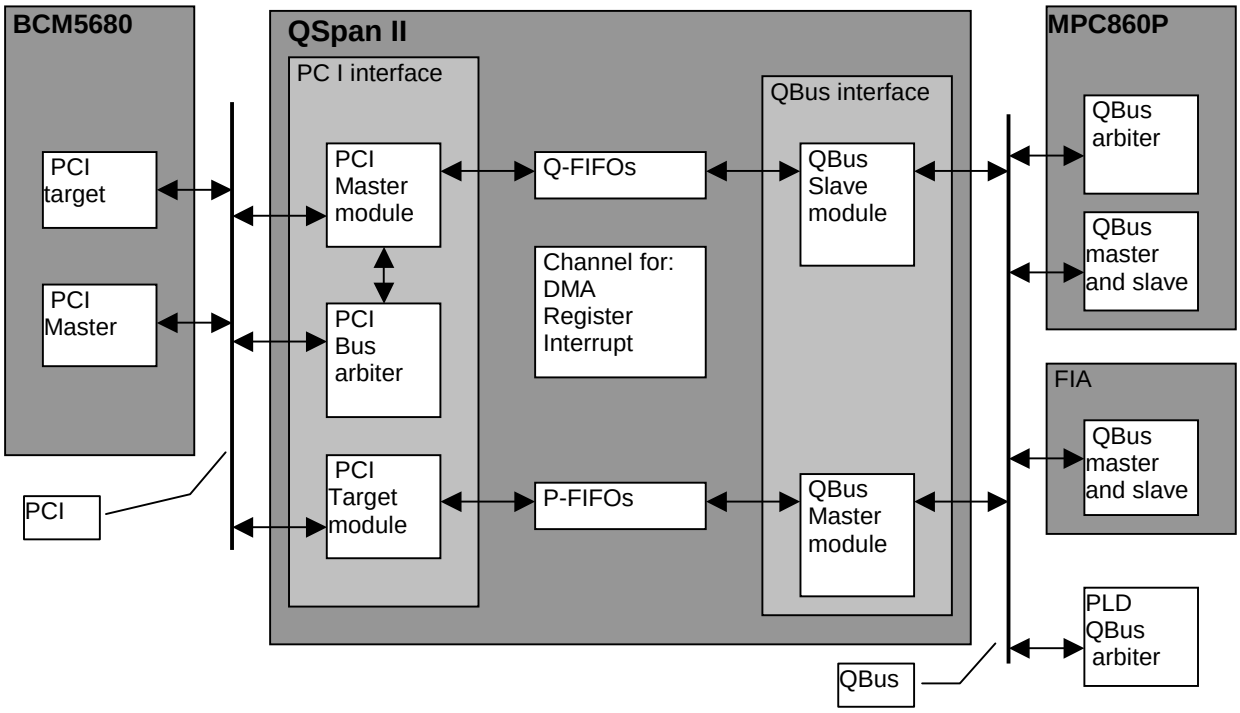

Figure 4: Block diagram of the Ethernet management

For this application (according to the figure above):

- QSpan II and BCM5680 both act as PCI Master and PCI Target.
- The PCI Bus arbiter functionality is within QSpan II.

The QBus arbiter functionality is within MPC860P at start-up. The MPC860 leaves after start-up the QBus arbiter to an external QBus arbiter (a PLD; see chapter 4.2.2.3).

- MPC860P, FIA and QSpan II are the QBus master and slave.

2.2.4.1 PCI bus (BCM5680 – QSpan II)

BCM5680

The PCI bus interface provided by the BCM5680 conforms to the PCI local Bus Revision 2.1 specifications. No external glue logic is required to support this interface.
In Layer 2 switching systems, the PCI interface is used for the set-up, configuration, maintenance, and management of the BCM5680 based switch system.
The BCM5680 supports the maximum PCI clock speed of 66 MHz on a 32-bit bus. The signalling of pins is for the 3.3V environment.

The BCM5680 supports both the PCI Target and PCI Master modes of operation.
As a target, it decodes 64 KB of memory address window for its internal memory and registers.
As a PCI master, the BCM5680 generates memory read and memory write cycles only on the PCI bus. It does not generate any I/O or configuration cycles.

QSpan II

QSpan II has a PCI Bus interface. The PCI interface connects the QSpan II to the PCI bus. The interface has two functional modules: a Master module and a Target module. A PCI bus arbiter is also included.
The QSpan II supports maximum 33 MHz operations on a 32-bit bus. The signalling of pins is for the 3.3V environment.

The chosen PCI operation frequency is the same as for the PHY-frequency: 25 MHz.

2.2.4.2 QBus

MPC860P and FIA at start up

The MPC860 QBus interface is both a master and a slave interface. The FIA is a master when a DMA transaction is taking place controlled by the FIA. FIA will utilise the bus arbiter, which is integrated in the PowerQUICC to become a master of the bus.

2.2.5 Power up, reset and initialisation

2.2.5.1 BCM5680

Power up and reset:

A power-on or hard reset is initiated by an active low reset pulse on the PCIRSTN input pin, and the RSTN signal from the PCI bus is used for this function. Internally a sufficiently long reset pulse is generated, which is applied to all the internal circuits.

Initialisation

Configuration via Management CPU:
In an unmanaged/managed switch the CPU can set-up the complete switch configuration by writing to appropriate configuration registers in the switch devices. The configuration can be changed during operation if necessary. However care has to be taken when writing to registers when traffic is going through the switch. It is recommended to read the appropriate registers (before writing to it) and write to the register only if some bits have to be changed.
The configuration of the switch is described in reference 22.

2.2.5.2 BCM5404

Power up and reset:
A hardware-reset pin (RESET active low) is provided, which reset all internal nodes inside the chip to a known state. The reset signal must be asserted for at least 2.0 µs. Hardware reset should always be applied to the BCM5404 after power-up.
The BCM5404 also has a software-reset capability.

Initialisation
Strapping pins: The switch devices read the configuration from strapping pins during reset see table below. Use the default internal pull-up and pull-down for configuration values that are final.
In this application the circuit is working in an auto-negotiation, full-duplex triple speed HUB (master) operating in GMII mode.
However at reset the circuit will be configured as a slave and DTE (data terminal equipment or “end station”) device.

Signals	I/O	Description	Implemented values at reset (pull-up or pull-down)
PHYA[4:0]	I_{PD}	PHY address select	PHYA[4:0] = [00001] : PHY 1-4: PHYA[4:0] = [00101] : PHY 5-8 See note 1.
FDX	I_{PU}	Full duplex select (active high) 1 = full duplex; 0 = half duplex	FDX = 1; see note 1 and note 4.
ER	I_{PD}	Edge Rate select 1 = the rise time is ≈ 5ns 0 = the rise time is ≈ 4ns	ER= 0; see note 2.
ANEN	I_{PU}	Auto-Negotiation select (active high). 1 = the BCM5404 performs auto-negotiation immediately after reset. 0 = auto-negotiation is disabled by default	ANEN = 1; see note 1 and note 4.
SPD0 F1000	I_{PD}	Speed select (active high). These pins set the default advertisement of the BCM5404 according to a table with the following signals: (WOL (Wake on LAN), ANEN, F1000, SPD0. If F1000 = 1 and ANEN = 1 then Auto-negotiation 10/100/1000BASE-T, No WOL. Se Datasheet table 1, label SPD0, F1000	SPD0 = 0 F1000 = 1; see note 1
EN_10B	I_{PD}	Enable 10 bit interface (active high) 1 = 10 bit interface, 0 = GMII	EN_10B = 0; see note 1.
MANMS	I_{PD}	Manual Master/Slave Configuration select (active high) 1 = Enable master/slave manual configuration value (se below HUB value) 0 = Automatic master/slave configuration	MANMS = 0; see note2.

Signals	I/O	Description	Implemented values at reset (pull-up or pull-down)
HUB{1} HUB{2} HUB{3} HUB{4}	I_{PD}	Repeater/Switch indicator (active high) 1 = Configure PHY as a master and Repeater/switch device port 0 = Configure PHY as a slave and DTE device	HUB = 0; see note 2.
WIRESPD	I_{PD}	Ethernet @ wire speed is a mode, which controls the auto-negotiation advertising. 1 = Enable wire speed mode 0 = Normal operation	WIRESPD = 0; see note 2.
RGMIIEN	I_{PD}	RGMII enable (active high) 1 = Use RGMII mode 0 = Normal GMII/MII operation	RGMIIEN = 0; see note 2.
EXTLPBK	I_{PD}	External loop-back enable (active high) 1 = External loop-back enabled 0 = Normal operation	EXTLPBK = 0; see note 2.
TEST[1:0]	I_{PD}	Test mode enables (active high). These pins must always be pulled low during normal operation	TEST[1:0]= [00] Leave open according to Broadcom.

Table 1 BM5404 strapping pins

Note 1: Use either internal or external pull-up or pull-down. If an internal pull-up is used, make it possible to mount an external pull-down. If an internal pull-down is used, make it possible to mount an external pull-up. After reset, the configuration is under software control.
Note 2: Internal pull-up or pull-down. After reset, the configuration is under software control.
Note 3: The PHY BCM5404 (with corresponding strapping pins) should work with together with the PHY BCM5401 (with corresponding strapping pins) on the SCB-RP board.
Note 4: According to errata (DOC#5404ER0.3C), there is an internal pull-down instead of an internal pull-up. Therefore an external pull-up is used.

2.2.5.3 Reset of QSpan II

QSpan II can be reset from the QBus or the PCI bus through hardware. QSpan II uses four pins and one register for reset options.

Pin name	Interface	Direction	Description
RST#	PCI	Input	Resets all the QSpan II circuits and registers and asserts RESETO_ when HS_HEALTHY is low. RESETO_ remains asserted until RST# is released. Also clears the SW_RST bit in the MISC_CTL register
RESETI_	QBus	Input	Resets most of the QSpan II circuits and registers. Not used in this application (pulled up)
RESETO_	QBus	Output	Resets devices on the QBus. Not used in this application.
HS_HEALTHY_	PCI	Input	This input indicates the state of the back-end system.

Table 2: QSpan II reset mechanism.

Initialisation

The following QSpan II configuration options can be determined at Reset (see table below):

- Whether the QSpan II is enabled as a PCI bus master.
- The mode of the QBus: master or slave.
- Whether the QSpan II loads registers from an EEPROM.
- Test mode.
- PCI access to QSpan II registers.
- PCI bus arbiter functionality.

Pin name	Interface	Direction	Description	Default values at reset (pull-up or pull-down)
BM_EN / FIFO_RDY_	PCI	Sampling at reset (Input)	*PCI Bus Master Reset Option:* If this pin is sampled high while reset is asserted, the QSpan II will set the Bus Master (BM) bit in the PCI_CS register. This enables the QSpan II as a PCI Bus Master. If this pin is not connected, an internal pull-down causes the QSpan II to power-up with the BM bit set to 0.	BM_EN/FIFO_RDY_ = 1 *PCI Bus master*
BDIP_ SIZ[1]	QBus	Sampling at reset (Input)	*Reset options for QBus Master and slaves modes*: QSpan II has four Master and Slaves modes that are determined by the BDIP_ and SIZ[1] signals at reset.	BDIP_ = X (don't care) SIZ[1] = 1 *Slave mode and MPC860*
ENID SDA		Sampling at reset (Input)	*Reset options for EEPROM loading of registers*: If either ENID or SDA is sampled high at reset, then the QSpan II will download register information from the EEPROM). No EEPROM is going to be used in this application	ENID = 0 SDA = 0 *No EEPROM loading*
TMOD[0] TMOD[1]		Sampling at reset (Input)	*Test mode*: For normal operations inputs must be pulled down	TMOD[0] = 0 TMOD[1] = 0 *Normal mode*
PCI_DIA		Sampling at reset (Input)	*PCI mode*: If PCI_DIS is sampled high at reset, the QSpan II will retry all PCI accesses until the PCI Access Disabled bit in MISC_CTL2 is set to 0 by the QBus processor For normal operations inputs must be pulled down	PCI_DIS = 0 *Normal mode*
PCI_ARB_EN		Sampling at reset (Input)	*PCI mode*: If PCI_ARB_EN is sampled high at reset the QSpan II´s PCI bus arbiter is enabled and will function as the PCI bus arbiter	PCI_ARB_EN = 1 *PCI bus arbiter*

Table 3: QSpan II initialisation.

2.2.6 Interrupts

The interrupts into the RPIHW1A_GESB module (to MPC860P) is the following:

Circuit	Pin name	To RPIHW1A_GESB module	Description
BCM5680 and QSpan II	INTA*	IRQ[7]	PCI interrupt. INTA* connected to both QSpan II and BCM5680.
QSpan II	QINT_	IRQ[6]	

Table 4: Interrupts to RPI module.

BCM5404

The BCM5404 can be programmed to provide an interrupt output based on changes in the PHY status. The conditions for which interrupts are provided are defined in the *Interrupt Status Register*.
However the *Interrupt Status register* has to be **polled to detect interrupts**.
Setting or clearing bits in the Interrupt Mask Register can individually mask interrupts. Most interrupts are cleared automatically by reading *the Interrupt Status Register*.
Setting the interrupt disable bit in the PHY Extended control register can globally disable the interrupt function.

BCM5680

The BCM5680 uses the INTA* line on the PCI bus to signal interrupts to the host CPU. Interrupts are generated for a variety of reasons, such as DMA operation complete, link status change, Global Buffer Pool full, ARL (address table) insert/delete operations, parity and fatal errors, I2C compatible operations, MIIM operations, etc.

QSpan II

QSpan II can generate interrupts based upon internal events provided that the interrupt source is enabled in the INT_CTL register. Interrupts can be mapped to an interrupt output pin on the PCI bus (INT#) or the QBus (QINT_) depending on the value of the interrupt mapping bit in the INT_DIR register.

2.2.7 Clocks

The switch part requires multiple clocks to perform the various operations. The clock and their frequencies are:

- *PCICLK* – input clock from the PCI bus interface, with 25 MHz for the PCI bus interface.
- *CORECLK* – 140 MHz input clock for the core logic of the device (maximum frequency of 142.8 MHz).
- *GMIICLKIN* - input clock to generate all the timings for the GMII and 8B/10B interface, with a frequency of 125 MHz
- *PHY* clock 25 MHz

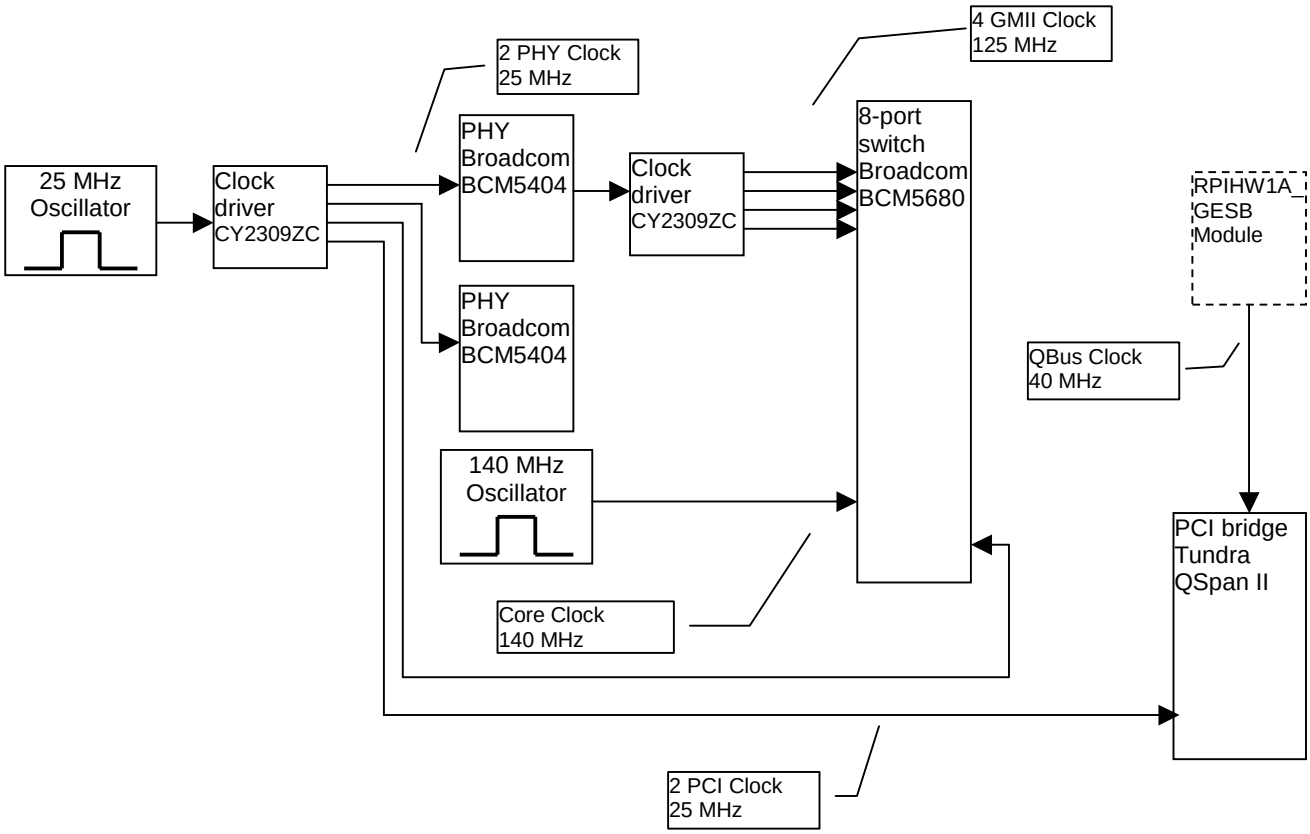

Figure 5: Block diagram of the clock distribution

2.3 RPIHW1A_GESB MODULE

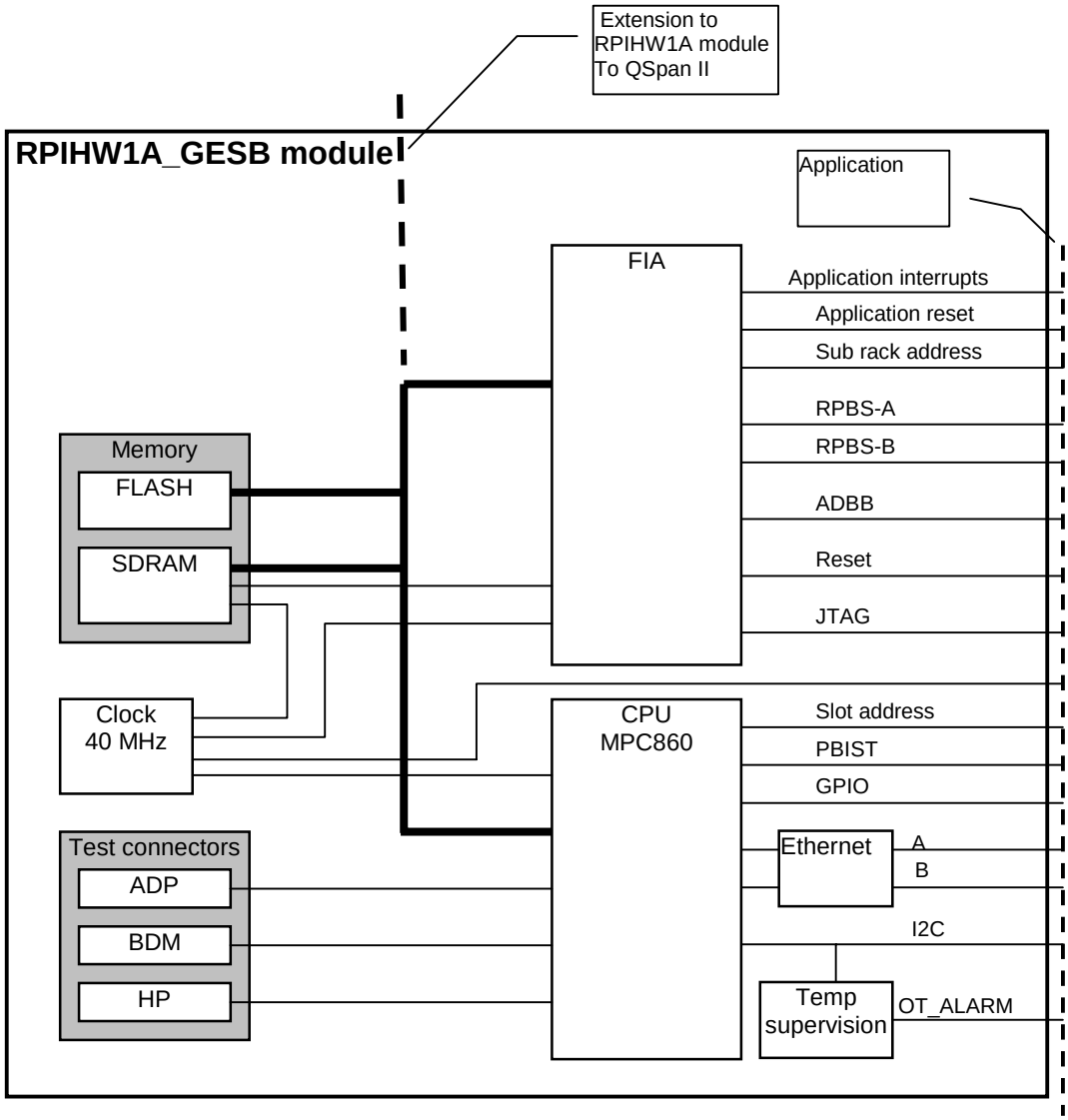

Figure 6: Block diagram of the RPIHW1A_GESB module

2.3.1 CPU

The processor is a MPC860P, which is an embedded processor from Motorola. It consists of a 32-bit PowerPC core and a communication processor module, which is controlled by a separate RISC processor.

2.3.2 FIA

This ASIC will be used as a companion chip to the MPC860 PowerQUICC communication controller.
FIA will have interfaces to the following functions/devices:

- The MPC860 bus with 32-bit address and 32-bit data
- IEEE 1149 JAG
- MTC IEEE 1149 JTAG (board master test controller)
- The serial RP-bus path A/B in back plane, RPB-S
- ADB (external devices with MPC860 interfaces connected through FIA)

2.3.3 Memory

The memory consists of Synchronous Random Access Memory (SDRAM) and Flash memory. The memory is connected via the 860-bus to the FIA and to MPC860.

2.3.3.1 Flash Memory

Flash memory size will be 8 megabyte. The Flash memory contains all program code for both operating system and application software. Before executing programs the code is copied to the SDRAM. In addition to the programs a number of parameters is stored in the Flashes.
After hard reset the system will boot from the Flash memory. The FIA drives a hard reset configuration word onto the system data bus. This will set the Boot Port Size to 32 bits. The MPC860 samples this word during reset.
The Flashes will be on-board programmed in production. JTAG is used to load the PBOOT part and Ethernet is used to load the OS.

2.3.3.2 SDRAM

32 megabytes of synchronous DRAM is used on GESB. 16 megabytes (4Banks x 1M x 32bit) will be used by software, both for program and data storage. The other half will be used for parity storage.

2.3.4 Ethernet

The RPIHW1A_GESB provides two standard 10Base-T Ethernet connections.

2.3.5 Clock in RPI.

A 40MHz-system clock is generated by an oscillator and feed to the MPC860 (the internal MPC860 system clock is however doubled to 80 MHz).
The MPC860s CLKOUT signal is connected to a zero delay clock driver with integrated PLL.
Two outputs of the clock driver can be used by applications outside the RPIHW1A_GESB. The PCI bridge, QSpan II, uses one of the outputs.

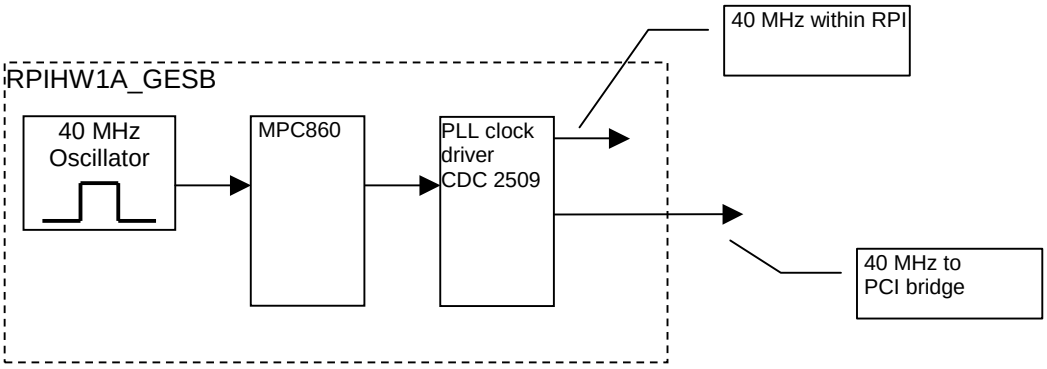

Figure 7: Block diagram of the 40 MHz clock distribution in RPI

2.3.6 Temperature Supervision

The RPI includes a digital temperature sensor with I2C interface (LM75).
The intention for the temperature sensor is to supervise the “hot spot” part of the PBA.
For this application the temperature sensor will be near the BCM5680 circuit.

2.3.7 Watchdog

The MPC860 includes a watchdog, which is used to generate a hard reset if it times out.

2.3.8 Timers

The MPC860 includes the following timers: Periodic Interrupt Timer, Power PC Decrement and Real-time clock.

2.3.9 Interrupts

Interrupts in RPIHW1A_GESB hardware module can be generated either internally or externally. Internal interrupts are generated from FIA or the MPC. External interrupts are generated from surrounding HW. The external interrupts can be used by the applications. They are connected to FIA.
The FIA is able to control interrupts from up to eight external sources. These external interrupts are available for the applications. The external interrupts are individually programmable for edge/level, low/high operation.
The Ethernet switch generates external interrupts, see chapter 2.2.6.

2.3.10 RPB-S

For communication with the CP in AXE, the GESB provides an RPB-S interface.

2.4 ADDITIONAL PARTS

2.4.1 Power

Board power is supplied for GESB from the back plane. The doubled -48V is connected together through protection diodes to the DC/DC converter.
The -48V will be converted to 3.3V, 2.5V and 1.8V respectively:

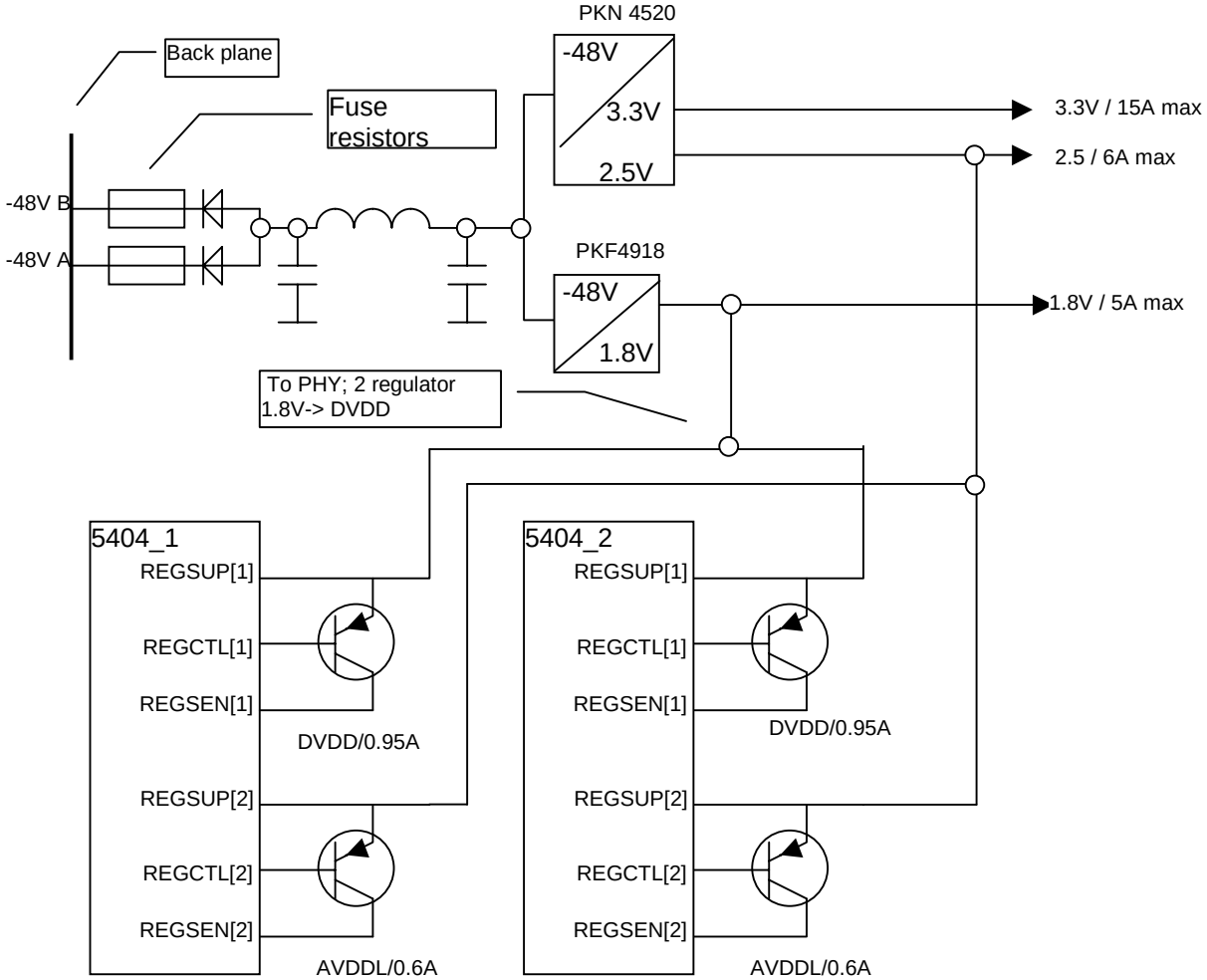

Figure 8: Power supply.

DC/DC conversion (from –48V):

- PKF 4918B SI: 1.8V / 5A (max).
- PKN 4520 API: 3.3V / 15A (max) and 2.5V / 6A (max) (max 50W).

Linear conversion (from 1.8V):

- BCM5404: DVDD; digital 1.2V / 1.9A needed (the voltage is programmable; default value is 1.2V). The regulator is internal and with external transistors.
- Regulator supply voltage (REGSUP[1]) is connected to 1.8V.

Linear conversion (from 2.5V):

- BCM5404: AVDDL; analogue 1.4V / 1.2A needed (the voltage is programmable; default value is for revision A0 on BCM5404 1.2V and for revision A2 1.4V). The regulator is internal and with external transistors.
- Regulator supply voltage (REGSUP[2]) is connected to 2.5V.

The internal regulator of BCM5404 uses an external PNP output current driver. Programming appropriate MII register bits can set regulator sense, REGSEN.

2.4.2 Reset

Power supply monitor for all secondary voltage (except AVDDL 1.4V analogue) is included on the GESB. The monitor for the 3.3V, 2.5V, 1.8V and 1.2V digital (DVDD) are three LTC1326-2.5 devices.
In case that any of the voltage drops below a specified threshold, the power reset is activated. It is connected to the power on reset input on the MPC860P (see figure below). This also forces drivers to the external world to be disabled.

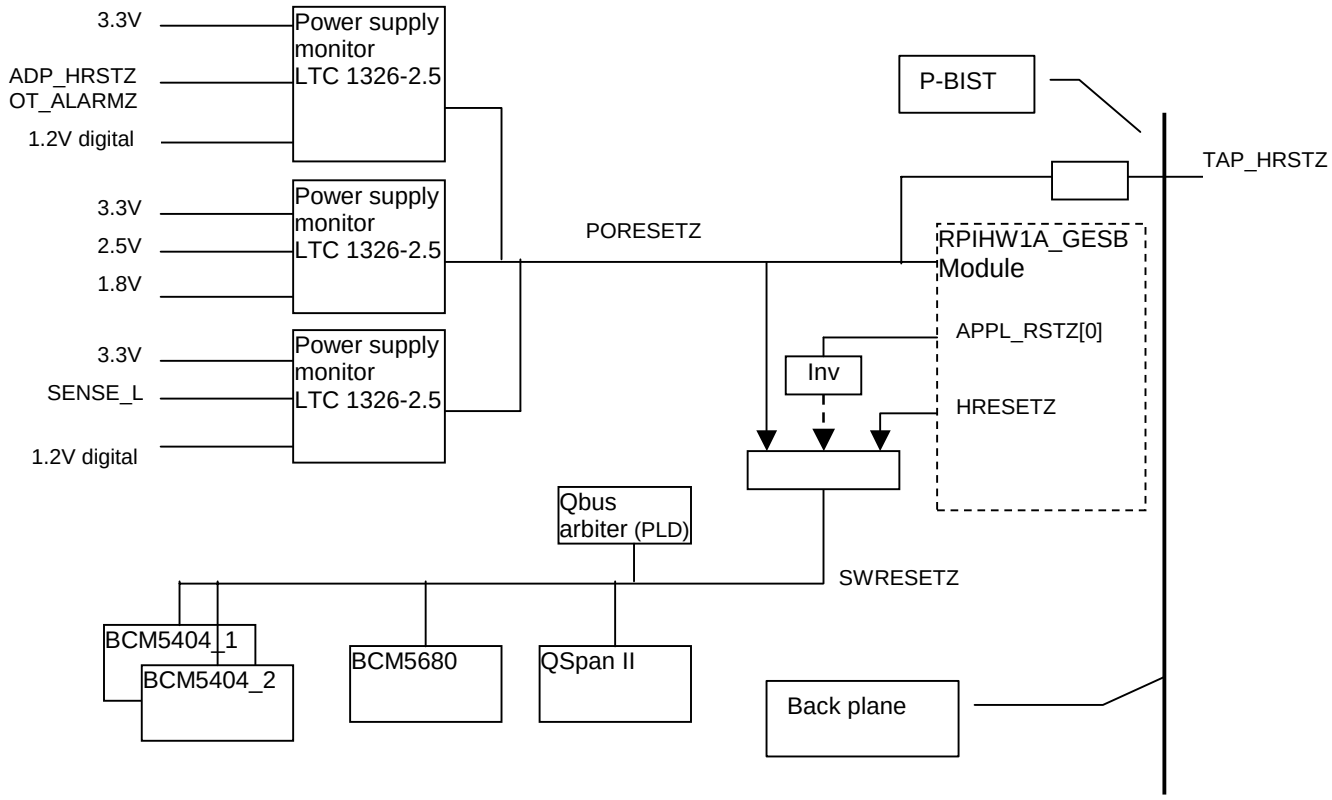

Figure 9: Voltage supervision and reset logic.

The main reset on the board is the power on reset (*PORESTZ*). This reset resets always all logic.
Power on reset (*PORESETZ*) will also cause the hard reset signal (*HRESETZ*) and the soft reset signal (*SRESETZ*) to be activated. The different reset levels and their sources are described below.
The switching part will be reset from a combined (AND) signal of PORESETZ, HRESETZ and an inverted APPL_RSTZ[0]: SWRESETZ (switch reset active low).
Note: APPL_RSTZ[0] is low at start-up. Therefore an inverter is included to APPL_RSTZ[0]. However this feature is disabled (a resistor is not mounted).

For each board there will be two back plane connectors, one in the top and one in the bottom that have shorter pins. The top-pin is connected (in the back plane) with one bottom-pin. All internal interfaces to/from the board must be inactive until both these pins are connected (top, bottom). See also reference 19, chapter 9.5.
In this application the signals SENSE_U and SENSE_L are used in the power supply monitor circuit.

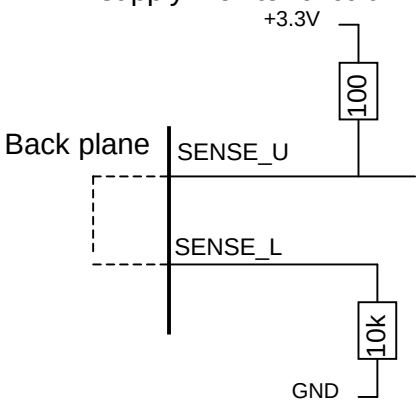

Figure 10: Shorter pins SENSE_U and SENSE_L .

There is no requirement of separate power supply to the power supply monitor. It is possible to use the voltage from the DC/DC converters.

Pin	I/O	Description	Application
V_{CC3}	I	3.3V sense input and power supply pin for the IC.	3.3V sense,
V_{CC25}	I	2.5V sense input.	2.5V sense, SENSE_L and combined OT_ALARMZ (over-temperature alarm) and ADP_HRSTZ (hard reset from the ADP)
V_{CCA}	I	1V sense; for higher voltage use a voltage divider	1.8V and 1.2V sense
RSTZ	O	Reset logic output. Active low, *open drain* logic output drives high to V_{CC3}. Asserted when one or more of the supplies are below trip thresholds and held for 200 ms after all supplies become valid.	Signal: PORESETZ (pull-up inside RPIHW1A_GESB).

Table 5: Power supply monitor LTC1326-2.5

2.4.2.1 Different reset levels

1. Sources of Power-on reset

- Power-on reset
- Over-temperature alarm
- Sense of board insertion
- ADP push button reset
- PBIST reset

2. Sources of Hard reset

- External hard reset (*HRESETZ* signal pin)
- Internal hard reset (PLL loss of lock, software watchdog
- Reset, check stop reset, debug port hard reset)
- Cold-start by command (from software)

3. Sources of Soft reset:

- External soft reset (*SRESETZ* signal pin)
- Internal soft reset (debug port soft reset)
- JTAG reset

2.4.3 Mbus

The GESB provides a slave maintenance bus interface like all other boards in the GEM magazine (see reference 19). This is implemented as a normal I^2C bus.
The maintenance bus also gives the possibility to point out specific boards in a magazine by controlling the MIA-LED.
The M-bus address for each slot is hard-coded in the back plane. An address pin connected to ground in the back plane = “0”. An open circuit address pin = “1”. Five address pins are used, which allow a maximum of 32 boards to be addressed. A0 is the least significant bit in the address.
Note: Slot address for physical addressing of the board and M-bus address do not use the same physical back plane pins, due to the separated power supply.

I^2C circuit	I^2C address **A6-A3 A2-A0** (A2-A0 hardware address pins on circuit)	R/W	Port	Description
PCF8574T	0100 MB_A2 – MB_A0	1 (read)	P0	MB_A3
		1 (read)	P1	MB_A4
			P2-P6	Not used
		0 (write)	P7	Output MIA-LED (from Mbus master).
X24C02S8	1010 MB_A2 – MB_A0	1 (read)	N.A.	Read HWID (from Mbus master).
		0 (write)	N.A.	Note: MBWCZ (write control signal for the Mbus slave) connected via a serial resistor to WC (write control) has to be active for writing. To be used by the production only to program the HWID.

Table 6: I^2C for Mbus

Note:

- X24C02S8: RYT 118 044/2C, 256 byte EEPROM in a SO8 package.
- PFC8574T: RYT 109 6048/3C, remote 8 bit I/O expander for I^2C bus in a SSOP20 package.

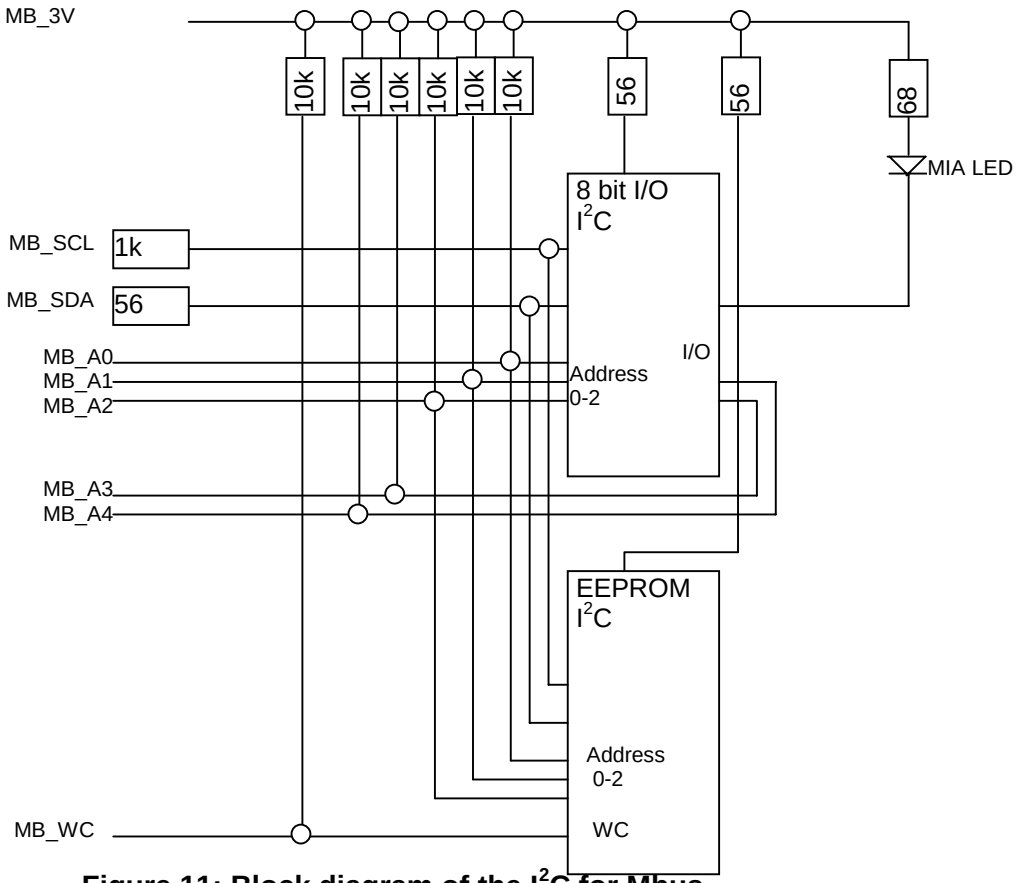

Figure 11: Block diagram of the I^2C for Mbus.

2.5 FUNCTIONAL MODES

2.5.1 Production Test Mode

The production can do functional tests of the components of RPIHW1A_GESB hardware module with P-BIST controlled by the on-board processor. P-BIST is mainly used for memory tests (RAM and Flash), FIA processor interface test and read/write operation to certain locations.
For production testing the GESB also provide a standardised JTAG interface. This inter-face allows connectivity tests between components as well as sampling and setting of chip I/Os.
In addition the JTAG interface is used by the production to load the boot and basic system programs into the Flash memory.

2.5.2 Operational Modes

2.5.2.1 Start Up Operation

MPC860 SPLL Power-on Reset Configuration
While the power on reset is active, the reset configuration of the SPLL of the MPC860 is sampled on the MODCK pins. On these pins the multiplication factor PLPRCR[MF] = ‘10’ is adjusted. Meaning the processor starts up with an internal frequency identical to the external oscillator frequency. Depending on the hard reset configuration word, the SCCR[EBDF] will be initialised to either ‘00’ or ‘01’ meaning the external bus will run at the internal frequency (full speed) or at the half speed respectively (see reference 14).
Hard Reset Configuration
When hard reset is active, a hard reset configuration word is driven by the FIA ASIC onto the data bus. The MPC860 determines its initial mode of operation by sampling the values present on the data bus (D[0-31]) during hard reset active.
The hard reset configuration word driven by FIA is shown in table 3.

Bits	Name	Value	Description
0	EARB	0	External ARBitration. Set to ‘0’ means internal bus arbitration is per-formed.
1	IIP	0	Initial Interrupt Prefix
2		0	Reserved
3	BDIS	0	Boot DISable. Is set to activate the memory controller so that it match all addresses
4	BPS	0	Boot Port Size. Is set to 32-bit port size.
5		0	
6	-	0	Reserved
7	ISB	1	Initial internal Space Base select. Defines the initial value of the IMMR bits 0-15 and determines the base address of the internal memory space.
8		0	
9	DBTGC	1	DeBuG pin Configuration. Configures the operation of a lot of signals (compare with “MPC860UM/AD Table 12.3”)
10		1	Reserved
11	DBPC	1	DeBug Port pins Configuration. Determines the active pins for the development port
12		1	
13	EBDF	0	External bus division factor. 00 Full speed bus. (01 Half speed bus.)
14		0	
15	-	0	Reserved

Table 7: Hard reset configuration word

2.5.2.2 Soft Reset Configuration

The rising edge of the SRESETZ signal is used to configure the development port (BDM). Before SRESETZ goes inactive, DSCK is sampled to determine for debug-mode enable/disable. After SRESETZ is disasserted, if debug mode was enabled, DSCK is sampled again for debug-mode entry/non-entry. DSDI is used to determine the debug port clock mode and is sampled after the negation of SRESETZ. The debug port controller provides the Soft Reset configuration.

2.6 MAINTENANCE

-

2.7 INDICATIONS AND ALARMS

There is an MIA LED in the front of the GESB, indicating that manual intervention is allowed when it lit.
The ADP interface controls three LED's that show the status of the boot procedure. This interface will only be used during debug and test.

2.8 SELF DIAGNOSTICS

The operating system is executing power up diagnostics and self-test after power up.

2.9 CONTROL FUNCTIONS

The RPI hardware module includes a temperature supervision circuitry. The used component, a LM75, is a temperature sensor and an over-temperature detector with I2C interface. The MPC860 can query the sensor via the I2C interface at any time to read temperature.
The open drain over-temperature shutdown output (OT_ALARMZ) becomes active (low) when the temperature exceeds a programmable limit. The processor is able to program both the temperature alarm threshold and the temperature at which the alarm condition goes away (hysteresis).
The assertion of the signal OT_ALARMZ will result in a power on reset. The GESB will be held in reset state until the temperature falls below the programmed threshold.
The thermostat settings for the board can be stored as parameters in the Flash. The OS can then read these values and program the thermostat registers after a power-on reset. If the OS does not program the thermostat, the default settings will be valid. This is 80°C alarm activating and 75°C deactivating (5° hysteresis) temperature threshold.
Note: The over-temperature shutdown cannot be disabled by software!

2.10 SYNCHRONISATION

There is no external synchronisation of the GESB necessary.

3 MEMORY MAP

Application	Size/width	Chip select	Address map
SDRAM	16 MB by 32 bit	CS1	0x0000 0000 – 0x00FF FFFF
FIA SRAM	512 kb		0xD000 0000 - 0xD007 FFFF
Dual Port RAM	16 kb		0xD700 0000 - 0xD700 3FFF
Ethernet switch			0xE000 0000 - 0xE0FF FFFF
FIA including device bus etc.			0xE100 0000 - 0xEFFF FFFF
QSpan II PCI Image 0 QSpan II PCI Image 1	64k by 32 bit 64k by 32 bit	CS2	0xF000 0000 - 0xF000 FFFF 0xF100 0000 - 0xF100 FFFF
QSpan II register space	1k by 32 bits	CS3	0xF200 0000 - 0xF200 0FFF
Flash	8MB by 32 bit	CS0	0xFF80 0000 - 0x10000 0000

Table 8: Memory map of the RPI

For detailed register description of the specific devices refer to reference 4, 10, 14 and 17.

4 ELECTRICAL REQUIREMENTS

4.1 EXTERNAL INTERFACES

The GESB is interfacing with external interfaces. These interfaces are described below.

RPIHW1A_GESB hardware module is interfacing with external interfaces. These interfaces are described below:

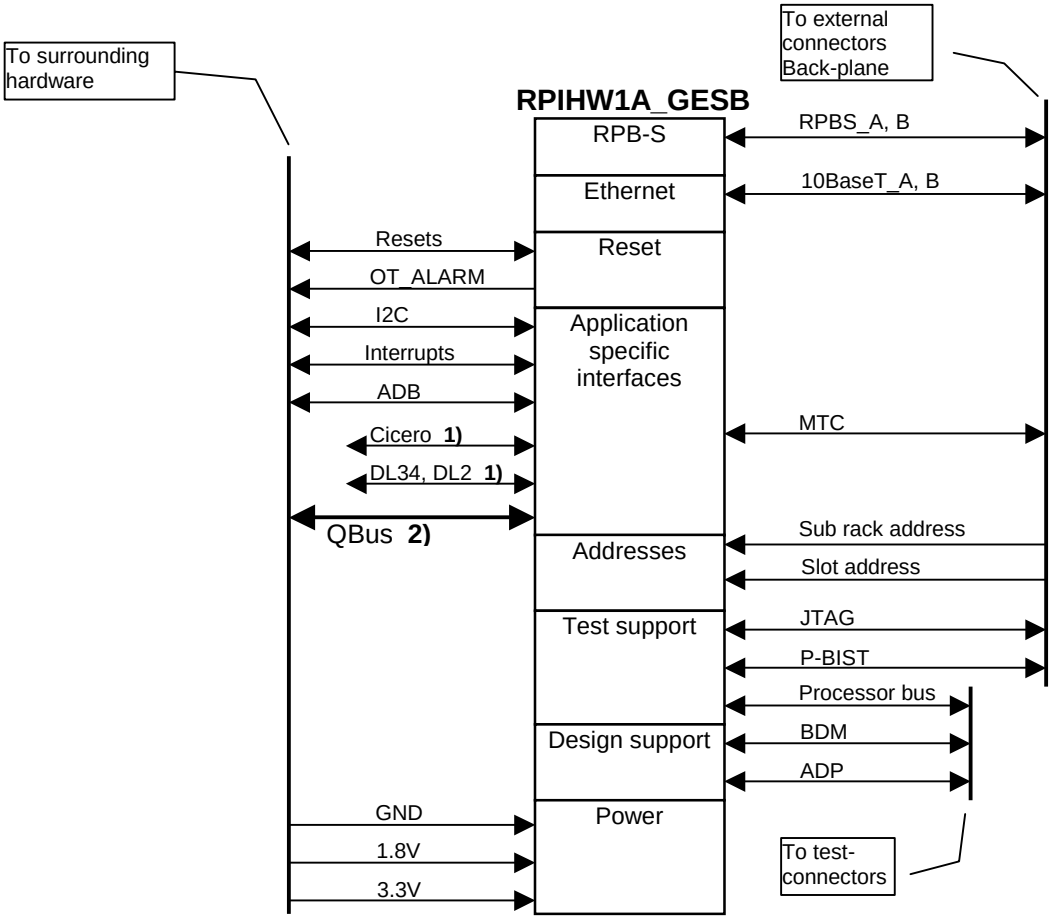

Figure 12: Overview of the RPIHW1A_GESB external interface.

1) Not used in GESB.
2) However for QBus interface additional signals is needed: Address, data and other signals (see chapter 4.2.2.2).

4.1.1 Front interfaces

Position	Signal name	Signal type	Width	In/Out	Description
X10y.A2 X10y.B1 y=0..7	TDP[0]{y} TDN[0]{y} y=0..7	1000-BaseT	2	I/O	Transmit Receive Pairs. In 1000Base-T mode, differential data from the media is transmitted and received on all four MX+/- signal pairs. In auto-negation, 10Base-T and 100Base-TX modes, MX_0 is transmitting and MX_1 is receiving pair. Auto-MDIX can reverse the pairs.
X10y.A3 X10y.B4 y=0..7	TDP[1]{y} TDN[1]{y} y=0..7	1000-BaseT	2	I/O	
X10y.A4 X10y.B3 y=0..7	TDP[2]{y} TDN[2]{y} y=0..7	1000-BaseT	2	I/O	
X10y.B2 X10y.A1 y=0..7	TDP[3]{y} TDN[3]{y} y=0..7	1000-BaseT	2	I/O	

Table 9: 1000Base-T - Gigabit Ethernet.

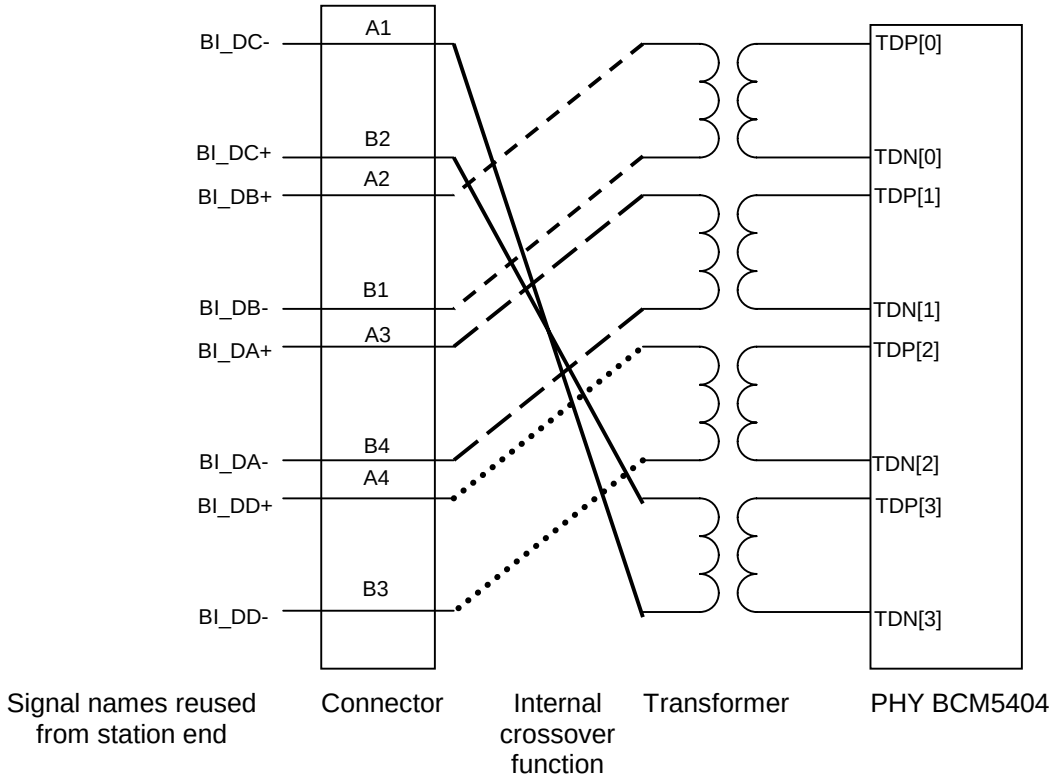

Figure 13: Overview of HUB/switch implementation.

The Ethernet interfaces are designed to connect a remote Ethernet station by using a plain one-to-on cable. This means the crossover function is implemented on the GESB (reference 6).

4.1.2 Back plane Interfaces

Position	Signal name	Signal type	Width	In/Out	Description
XP01.01 – XP01.04	GND	Power feed	4	I	GND Branch A
XP01.05 – XP01.08	-48V_A	Power feed	4	I	-48V Branch A
XP02.01 – XP02.04	GND	Power feed	4	I	GND Branch B
XP02.05 – XP02.08	-48V_B	Power feed	4	I	-48V Branch B

Table 10: -48V Power Supply.

Position	Signal name	Width	Description
X01.A01	SENSE_U	1	Sense upper (SENSE_U and SENSE_L is connected in back plane)
X11.A10	SENSE_L	1	Sense lower

Table 11: Short pin-out.

Position	Signal name	Signal type	In / Out	Description
X01.A02	MB_A0	GND or open	I	Address pins for the Mbus. This same information as board addresses but is electrically separated in the back plane.
X01.B02	MB_A1		I	
X01.D02	MB_A2		I	
X01.E02	MB_A3		I	
X01.A03	MB_A4		I	
X01.B03	MB_SDA	LV-CMOS	I/O	Serial data for the Mbus slave
X01.A04	MB_SCL	LV-CMOS	I	Serial clock for Mbus slave.
X01.B01	MBWC	LV-CMOS	I	Write Control signal for the Mbus slave. To be used by the production only to program the HWID
X01.B04	MB_3V		I	3.3V Power Supply for the Mbus slave on GESB.

Table 12: Mbus slave interface.

Position	Signal / RPI symbol name	Signal type	In / Out	Description
X10.B09	RPB_MA_TX / RPBS[5]	LV-CMOS	I	RPBS receive data from CP to RP on path A.
X10.B10	RPB_MA_RX / RPBS[3]		O	RPBS receive data from RP to CP on path A
X10.D09	RPB_MB_TX / RPBS[4]		I	RPBS receive data from CP to RP on path B.
X10.D10	RPB_MB_RX / RPBS[2]		O	RPBS receive data from RP to CP on path B

Table 13: RPB-S back plane interface.

Position	Signal / RPI symbol name	Signal type	In / Out	Description
X11.D03	BADR-S0 / B_ADR[0]	GND or open	I	Board address, hard-coded in the back plane. The board address is connected to some of the MPC860's GPIOs. It is used for calculating the RP address
X11.E03	BADR-S1 / B_ADR[1]		I	
X11.A04	BADR-S2 / B_ADR[2]		I	
X11.B04	BADR-S3 / B_ADR[3]		I	
X11.D04	BADR-S4 / B_ADR[4]		I	
X11.E04	BADR-SP / B_ADR[5]		I	Odd parity calculated from the BADR-S0-BADR-S4. The board address parity is connected to one of the MPC860's GPIOs
X10.A06	AP_0-S0 / SR0ADR[0]	GND or open	I	Magazine address taken from AP-0 used for physical RP address calculation. The sub rack address is connected to the FIA ASIC
X10.B06	AP_0-S1 / SR0ADR[1]		I	
X10.D06	AP_0-S2 / SR0ADR[2]		I	
X10.E06	AP_0-S3 / SR0ADR[3]		I	
X10.E05	AP_0-SP / SR0ADR[4]		I	Even Parity calculated from AP_0-S0 - AP_0-S3. The sub rack address parity is connected to the FIA ASIC
X11.A01	AP_1-S0 / SR1ADR[0]	GND or open	I	Address taken from AP-1 used to indicate the magazine start address (column). The sub rack address is connected to the RPI module (FIA ASIC)
X11.B01	AP_1-S1 / SR1ADR[1]		I	
X11.D01	AP_1-S2 / SR1ADR[2]		I	
X11.E01	AP_1-S3 / SR1ADR[3]		I	
X11.A02	AP_1-SP / SR1ADR[4]		I	Even Parity calculated from AP_1-S0 - AP_1-S3. The board address parity is connected to the RPI module (one of the MPC860's GPIOs)
X11.B02	AP_3-S0 / SR3ADR[0]	GND or open	I	Address taken from AP-3 used to indicate the magazine start address (row). The sub rack address is connected to the RPI module (FIA ASIC)
X11.D02	AP_3-S1 / SR3ADR[1]		I	
X11.E02	AP_3-S2 / SR3ADR[2]		I	
X11.A03	AP_3-S3 / SR3ADR[3]		I	
X11.B03	AP_3-SP / SR3ADR[4]		I	Even Parity calculated from AP_3-S0 – AP_3_S3. The board address parity is connected to the RPI module (one of the MPC860's GPIOs)

Table 14: Addresses.

The implementation of the addresses: see reference 19.

Position	Signal / RPI symbol name	Signal type	In / Out	Description
X10.A01	10BaseTA_TXP / 10BASET_IO[0]	10BASE-T	O	Transmit Data A Transmit Differential Pair. These pins transmit the serial bit-stream. The differential pair is a 2 level signal in 10Base-T mode. These signals are isolated via a transformer
X10.B01	10BaseTA_TXN/10 BASET_IO[1]			
X10.A02	10BaseTA_RXP / 10BASET_IO[2]		I	Receive Data A Receive Differential Pair. These pins receive the serial bit bit-stream. The differential pair is a 2 level signal in 10Base-T mode. These signals are isolated via a transformer.
X10.B02	10BaseTA_RXN/10 BASET_IO[3]			
X10.D01	10BaseTB_TXN/10 BASET_IO[5]		O	Transmit Data B
X10.E01	10BaseTB_TXP / 10BASET_IO[4]			
X10.D02	10BaseTB_RXN / 10BASET_IO[7]		I	Receive Data B
X10.E02	10BaseTB_RXP / 10BASET_IO[6]			
X10.B05	EA_SRE / ELIFA[1]	LV-CMOS		SR enable A (Ethernet lite, slave pin out E_SRE reference 19, chapter 9.7.3)
X10.D05	EB_SRE / ELIFB[1]	LV-CMOS		SR enable B

Table 15: Ethernet slave and Ethernet support.

4.1.2.1 JTAG

The JTAG interface is used during the manufacturing to load the boot program into the flash memory. This interface will also be used to perform boundary scan tests on the PBA. The signals of the JTAG interface are connected to the back plane.

Position	Signal / RPI symbol name	Signal type	In / Out	Description
X11.B06	JTAG1_TMS	LV-CMOS	I	Test Mode Select
X11.D05	JTAG1_TDI	LV-CMOS	I	Test Data In
X11.D06	JTAG1_TDO	LV-CMOS	O	Test Data Out of the FIA.
X11.A06	JTAG1_TRSTZ	LV-CMOS	I	Test ReSeT (low active) *.
X11.B06	JTAG1_TCK	LV-CMOS	I	Test Clock
X01.E03	JTAG2_TMS / ASP_BUS[2]	LV-CMOS	I	ASP Test Mode Select
X01.D03	JTAG2_TDI / ASP_BUS[3]	LV-CMOS	I	ASP Test Data In
X01.D04	JTAG2_TDO / ASP_BUS[4]	LV-CMOS	O	ASP Test Data Out of the FIA.
X01.E01	JTAG2_TRST / ASP_BUS[0]	LV-CMOS	I	ASP Test ReSeT (low active) *.
X01.D01	JTAG2_TCK / ASP_BUS[1]	LV-CMOS	I	ASP Test Clock
X01.E04	ASP_BYPZ / ASP_BUS[5]	LV-CMOS	I	By pass
X11.B10	MTC_TMS / MTC[2]	LV-CMOS	I	MTC Test Mode Select
X11.D10	MTC_TDI / MTC[1]	LV-CMOS	I	MTC Test Data In
X11.E05	MTC_TDO / MTC[0]	LV-CMOS	O	MTC Test Data Out of the FIA.
X11.A05	MTC_TRSTZ / MTC[4]	LV-CMOS	I	MTC Test ReSeT (low active) *.
X11.A09	MTC_TCK / MTC[3]	LV-CMOS	I	MTC Test Clock

Table 16: JTAG.

It is recommended by Motorola to combine TRSTZ signal of the processor with the power on reset signal or to ground TRSTZ during normal operation.

4.1.2.2 PBIST

P-Bist interface gives the possibility to do built in self-tests of processor and the memory system.
The P-BIST interface on GESB is designed to meet the requirements for P-BIST (see reference 12).

Position	Signal / RPI Symbol name	Signal type	In / Out	Description
X11.D08	TMPZ0 (TMPZ, PA_6) / PBIST[0]	LV-CMOS	I	P-Bist Test Mode Pin.
X11.E08	TMPZ1	LV-CMOS	I	Test Mode Pin 1. Not used .
X11.B07	TRG (PA_7) / PBIST[1]	LV-CMOS	O	P-Bist Trigger.
X11.B09	V24_TX (PD_8) / V24_1_BP[0]	RS232	O	V24 transmit/receive data (RS-232 interface used for communication between MPC860 (SCC4) and the external test equipment.
X11.D09	V24_RX (PD_9) / V24_1_BP[1]	RS232	I	
X11.E06	FWZ / TEST[3]	LV-CMOS	I	JTAG Flash write
X11.D07	FWPEZ / TEST[5]	LV-CMOS	I	Flash Write Protect enable
X11.A08	P3V	Power feed	I	+3.3V (P3V and PGND can be used for external drivers (V24). On the PBA, 10 ohm shall be put in series with 3.3V).
X11.B08	PGND	Power feed	I	GND
X11.A07	TAP_HRSTZ	LV-CMOS	I	External hard reset; see chapter 2.4.2 Reset
X11.E10	Vcc_mon	Power feed	I	Extra voltage monitor (If Vcc_mon is used, a resistor shall be put in series). Not used.

Table 17: Other signals (TAP and P-BIST).

The test access port is the interface towards PBA production test (P-BIST).

4.1.3 External test interfaces on board

These additional test interfaces are not available in the front or in the back plane connectors. The connector is located on the board, but will not be equipped on the released product. See reference 4 for more information.

ADP

The Advanced Debug Port (ADP) interface is used for debugging during both design verification and software development.

BDM

The Background Debug Mode (BDM) interface is used for debugging during both design verification and for software development. It provides a full duplex serial interface between the MPC860's core and an external development tool.

4.1.4 Additional external test interfaces on board

The PCI signals (both address/data and other signals), QBus arbiter signals and Ethernet management signals (see 4.2.1 MDC and MDIO) will be provided on two Tektronix connectors.

These connectors will be used only during test and they will not be equipped on the released product.

4.2 INTERNAL INTERFACES

4.2.1 Ethernet Management interface: PHY

Management of BCM5404:
The BCM5404 contains a set of management registers. The status and control registers of the BCM5404 are accessible through the MDIO and MDC serial interface. The functional and electrical interface is compliant to IEEE 802.3 (section 22) and also supports increased MDC clock rates up to 12.5 MHz. The management interface supports the defined status and control registers of IEEE 802.3, 802.3u (sections 22 and 40). In addition, the BCM5404 contains multi-purpose registers for easy management software design.

4.2.2 Ethernet Management interface: 8-port switch

Management of BCM5680:
The Ethernet Management Interface allows communication between the MPC860 and the Ethernet switch devices.
It connects the PCI bus from the BCM5680 to the address/data bus of the CPU.

4.2.2.1 PCI bus (BCM5680 - QSpan II).

The table below shows the various PCI bus interface signals (see reference 16 and reference 17, chapter 16.6).
.

BCM5680	QSpan II	Pull-up pull-down	Description
PCI_AD[31:0]	AD[31:]		PCI Address/Data Bus: address and data are multiplexed over these pins providing a 32-bit address/data bus. A bus transaction consists of an address phase followed by one or more data phases.
/C_BE[3:0]	C/BE#[3:0]		PCI Bus Command and Byte enable: command information during address phase and byte line enables during data phase.
PAR	PAR		Parity: parity is even across AD[31:0] and C/BE#[3:0]
/FRAME	FRAME#	PU	Beginning and duration of an access.
/IRDY	IRDY#	PU	Initiator ready
/TRDY	TRDY#	PU	Target ready
/STOP	STOP#	PU	Stop signal
/DVSEL	DEVSEL#	PU	PCI Device select. Sampled by the QSpan II when it is PCI master.
IDSEL	IDSEL		Initialisation Device select: BCM5680 AD16; QSpan II pull-down
/PCIRST	RST#		PCI reset
PCICLK	PCLK		PCI bus reference Clock
/GNT	GNT#		PCI Grant
/REQ	REQ#	PU	Bus Request
/SERR	SERR#	PU	System error.
/PERR	PERR#	PU	Parity error.
/INTA	INT#	PU	Interrupt

Table 18: PCI Interface signals

4.2.2.2 QBus (QSpan II – RPIHW1A_GESB/MPC860P).

The table below shows the various QBus interface signals (see reference 16 Appendix C.2).
1) In the table below new signals is needed for the RPIHW1A_GESB symbol.
2) Some signals have been investigated carefully (no disturbance to RPI functionality): CS2, CS3, IMSEL, IRQ4, DSDI, and DSCK.

Signal / RPI symbol name	QSpan II name	Pull-up pull-down	Description
CLK_0 / CLK[6]	Q_CLK		To QSpan II. Buffered 40 MHz clock.
CS2 **2)**	Q_CSPCIZ		To QSpan II. QSpan II requires that two chip selects be generated in order to access the registers (CSREG_) and the PCI bus (CSPCI_). This can be accomplished by using two of the chip select outputs from the memory controller within the MPC860.
CS3 **2)**	Q_CSREGZ		
A[0:31] / **A[0:31] 1)**	A[31:0]		Address bus. ***Note MSB/LSB***. **New RPIHW1A_GESB signals**.
Use one GPIO: PB14 / PB[0] **2)** (this port is reserved for application)	Q_IMSEL		To QSpan II. There are two QBus slaves images within the QSpan II, which are used to access the PCI bus. The image that is selected when the PCI chip select is asserted is dependent on the state of the Image Select signal (IMSEL). If IMSEL is low then the QBus slave image 0 is selected; otherwise, QBus slave image 1 is selected. IMSEL is typically generated directly from one of the high order address lines on the QBus (for example dependent of the processor's memory map).
D[0:31] / **D[0:31] 1)**	D[31:0]		Data bus. ***Note MSB/LSB***. **New RPIHW1A_GESB signals**.
DP[3:0] / **DP[3:0] 1)**	Q_DPAR[0:3]		Data parity. ***Note MSB/LSB.*** **New RPIHW1A_GESB signals**.
TSIZ0 / PQ_CTRL[4]	Q_SIZ1	PU	***Note MSB/LSB***.
TSIZ1 / PQ_CTRL[5]	Q_SIZ0	PU	***Note MSB/LSB.***
TSZ / PQ_CTRL[8]	Q_TSZ	PU	
RDWRZ / PQ_CTRL[0]	Q_RD_WRZ	PU	
BDIPZ / PQ_CTRL[7]	Q_BDIPZ	PU	BDIP_ must be pulled up for 860 master mode.
BURSTZ / PQ_CTRL[6]	Q_BURSTZ	PU	
BRZ / PQ_CTRL[1]	QSPAN_BRZ		To external QBus arbiter
BGZ / PQ_CTRL[2]	QSPAN_BGZ		To QSpan II
BBZ / PQ_CTRL[3]	Q_BBZ	PU	Bus Busy: indicates ownership of the QBus. BB_ is asserted low by a master to show that it owns the bus.
TEAZ / PQ_CTRL[10]	Q_TEAZ	PU	
IRQ4 **2)**	Q_RETRYZ	PU	
TAZ / PQ_CTRL[9]	Q_TAZ	PU	
N/A	TC3		Transaction Code Bus: As a slave, the QSpan II samples TC[3:0] on the first rising edge of the QCLK after TS_ is asserted. Note MSB/LSB. Not used.
N/A	TC2		
N/A	TC1		
N/A	TC0		
K17/PB23 / PB[5] (note reserved for future use RPI)	Q_SDACKZ	PU	To QSpan II
D16/PC15 / PC[2] (reserved for application)	Q_DREQZ		To MPC860P
IRQ6	Q_INTZ	PU	
SWRESETZ	RST#	PU	To QSpan II. Combined PORESETZ and HRESETZ signal; see chapter 2.4.2
N/A	RESIZ	PU	Pull-up at QSpan II.
N/A	DSACK0Z DONEZ ENID SDA ASZ	PU PU PD PD PU	Pull-up at QSpan II.

Table 19: QBus Interface signals

4.2.2.3 External QBus arbiter

There are three masters on the QBus: MPC860, FIA and QSpan II. MPC860 can only handle two masters. Due to three masters on the QBus an external QBus arbiter is needed. This arbiter is within a PLD from Altera.

At power up, the internal arbiter of MPC860 for the QBus (MPC-bus) is active. Only MPC860P and FIA are masters. The BRZ and BGZ signals from the FIA and MPC860P are connected together (within the external arbiter).

After power up, the MPC860 handle over the arbiter function to the external device (ARB_ENABLE = 1 and internal EARB=1). After that also the QSpan II has the possibility to be master on the QBus.
The table below shows the signal needed for the external arbiter.

Signal/Pin	In/Out	Description
ARB_CLK / 37 (GCLK1)	In	40 MHz clock
RESETZ / 39 (GCLR)	In	Active low reset signal
Enable / 38 (OE1)	In	Active high enable signal (external pull up)
Enable / 40 (OE2)	In	Active high enable signal (external pull up)
Q_BBZ / 27	In	QBus; Bus busy From MPC860, FIA or QSpan II
ARB_ENABLE / 25	In	ARB_ENABLE = 1 PLD is the external arbiter ARB_ENABLE = 0 MPC860P is the arbiter. Signal from MPC860P.
CPU_BRZ / 20	In/Out	MPC860P Bus request. Input if ARB_ENABLE = 1 ; from CPU Output if ARB_ENABLE = 0; to CPU (CPU_BRZ = FIA_BRZ)
CPU_BGZ / 21	In/Out	MPC860P Bus request. Output if ARB_ENABLE = 1 ; to CPU Input if ARB_ENABLE = 0; from CPU (FIA_BGZ = CPU_BGZ)
FIA_BRZ / 18	In	From FIA; Bus request
FIA_BGZ / 19	Out	To FIA; Bus grant
QSPAN_BRZ / 22	In	From QSpan II; Bus request
QSPAN_BGZ / 22	Out	To QSpan II; Bus grant
TDO / 32	Out	JTAG signal
TDI / 1	In	JTAG signal
TMS / 7	In	JTAG signal
TCK / 26	In	JTAG signal

Table 20: QBus arbiter signals

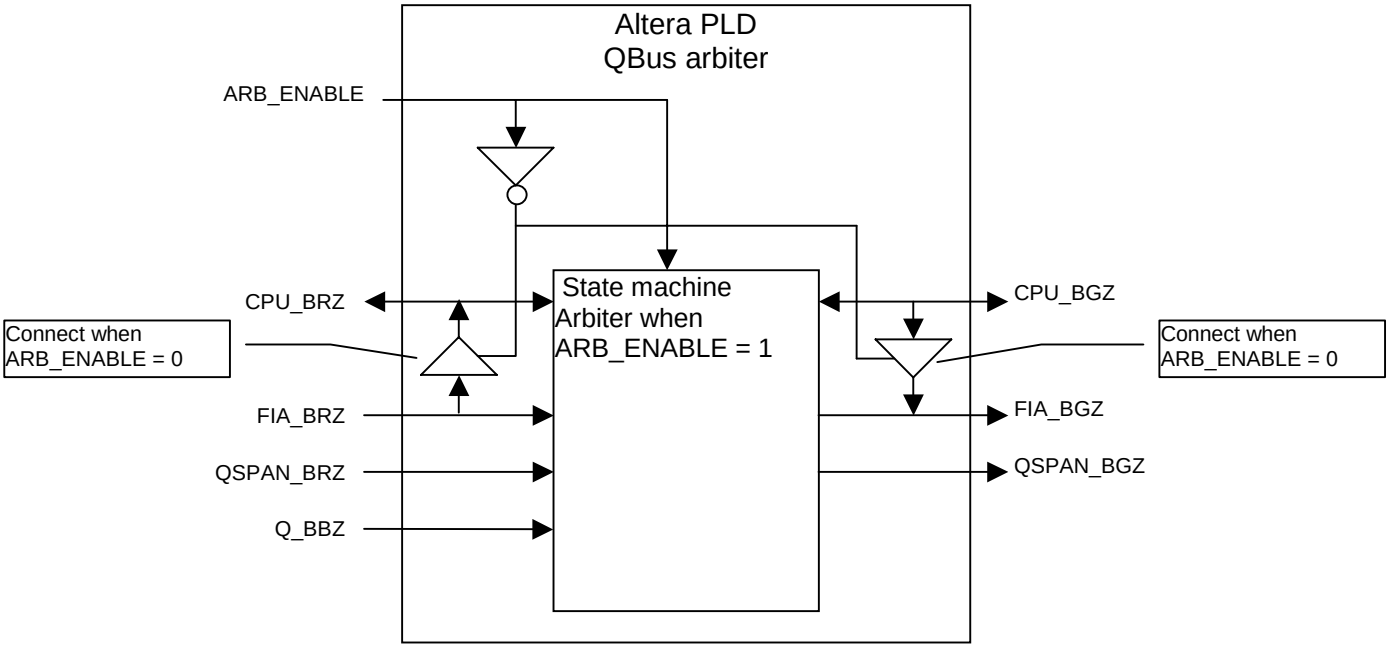

Figure 14: QBus arbiter block diagram.

4.2.3 GMII

The GMII (Gigabit Media Independent Interface) is the digital data interface between the MAC and the physical layer when operating in 1000BASE-T mode. The transmit signals include TX_EN, GTX_CLK, TXD[7:0], and TX_ER. The receive signals include RX_DV, RX_CLK, RXD[7:0] and RX_ER. The media status signals include CRS and COL.
The GMII is extended from the MII to use 8-bit data interfaces and to operate at higher frequency (125MHz). Most of the signals are physically shared with the MII interface.
The management interface is the same in both MII and GMII.

4.2.4 MII

The MII (Media Independent Interface) is a subset of the GMII and is the digital data interface between the MAC and the physical layer when operating in 10BASE-T and 100BASE-TX modes. The BCM5404 MII contains all the signals required to transmit and receive data at 10Mbps and 100Mbps speeds for both full and half-duplex operation. The transmit signals include TX_EN, TX_CLK, TXD[3:0], and TX_ER. The receive signals include RX_DV, RX_CLK, RXD[3:0] and RX_ER. The media status signals include CRS and COL.

4.3 USAGE OF GPIOS OF THE MPC860.

The MPC860's communication processor module (CPM) supports four general-purpose I/O ports - A, B, C, and D. Each signal in the I/O ports can be configured as a general-purpose I/O signal or as a signal dedicated to supporting communications devices, such as SCCs or SMC's. The tables in reference 4 show the usage of the I/O ports.

There are a number of spare GPIOs (see reference 4) that are either marked with 'reserved for RPI 'or' for application'. No pull up resistors is provided on those pins. Therefore it has to be ensured by the OS or the application software that those unused GPIOs are configured as outputs.

4.4 ETHERNET PORT MAPPING

The following table shows how the external Ethernet ports are assigned to the specific integrated circuits.

Front connectors		Switch device	5 bit PHY address	PHY device port
X221	**Port 7**	5404-1	00001	**1**
X222	**Port 6**	5404-1	00010	**2**
X223	**Port 5**	5404-1	00011	**3**
X224	**Port 4**	5404-1	00100	**4**
X225	**Port 3**	5404-2	00101	**5**
X226	**Port 2**	5404-2	00110	**6**
X227	**Port 1**	5404-2	00111	**7**
X228	**Port 0**	5404-2	01000	**8**

Table 21: Ethernet Port Mapping.

Note the numbering of the front connectors and the PHY device ports (see also chapter 2.2.

4.5 POWER SUPPLY

An estimation of max power dissipation (from reference 5) is 42W/ 30 mm width.

The GESB requires four different voltages to be supplied:
+3.3V is needed for all logic and I/O (all RPIHW1A_GESB except FIA, BCM5680. BCM5404, QSpan II etc.). The current needed is about 2.4 A
+2.5V is needed for the BCM5680 and BCM5404. It is used for the core supply of the Ethernet switch components. The current needed is about 5 A.
+1.8V is only needed for the core supply of the FIA ASIC. No other logic requires this +1.8V supply. The current needed is about 200 mA. Note this voltage is linear regulated from 2.5V.
+1.4V is only needed for the BCM5404 (analogue parts). No other logic requires this +1.4V supply. The current needed is maximum 1.2 A. This voltage is linear regulated from 2.5V.
+1.2V is only needed for the BCM5404 (core supply. No other logic requires this +1.2V supply. The current needed is maximum 1.9 A. This voltage is linear regulated from 1.8V.

Part	**Voltage/current**			**Power dissipation**	**Comments**
	1.8 V	**2.5 V**	**3.3 V**		
RPIHW1A_GESB	0.2 A		1.2 A	4.32 W	
Various (voltage supervision)			0.15 A	0.5 W	Assumption 0.15 A
8-port switch (BCM5680 and QSpan II)		3.04 A	0.48 A	9.2 W	
PHY (BCM5404)	1.9 A	3.15 A	0.52 A	13 W	Linear regulation 1.8V -> digital 1.2V; 2.5V -> analogue 1.4 V
Total current	**2.1 A**	**6.2 A**	**2.35 A**		
Total power dissipation				**30 W**	Inclusive DC/DC converter efficiency (90%)

Table 22: Power dissipation of the GESB.

The total power consumption of the GESB is estimated to be maximum 30 Watts. These values are based on the values from data sheets and estimated values.

5 COMPONENTS

The main components that shall be used are listed in table.

Part	Component	Type /Vendor	Product number	Package	Qty
RPIHW1A_GESB					
	CPU	MPC860P / Motorola	RYT 123 6085/1	PBGA 357	1
	FIA	ASIC / TI	ROP 101 12	BGA 432	1
	SDRAM	KM416S4030AT / Samsung	RYT 119 106/C	TSOP 54 (II)	4
	Flash	RC28F320C3 / Intel	RYT 118 6152/4	EBGA64	2
	10Base-T PHY	LXT905 / Level One	RYT 121 159/2C	LQFP32	2
	Oscillator 40 MHz ±100ppm		RTL 201 028/17		1
	PLL clock driver	CDC2509 / TI	RYT 109 6141/C		1
Additional					
	DC/DC converter	PKN 4520 API/ Ericsson	RYT 913 115/3		1
	DC/DC converter	PKF 4918B SI/ Ericsson	RYT 913 6003/2		1
	Power supply monitor	LTC 1326-2.5 / Linear Technology	RYT 113 6229/1		3
	Transistor, PNP	BDP32 / Philips	RYN 120 659/1	SOT223	4
	EEPROM	X24C02S8	RYT 118044/2C	SO8	1
	I2C expander	PFC8574T	RYT 1096048/3C	SSOP20	1
	Connector position XP01, XP02 and X01	Teradyne	RNV6401151/18		1
	Connector position X10 and X11	Teradyne	RNV6401151/19		1
Gigabit Ethernet switch					
	8-port Gigabit switch	BCM5680 / Broadcom	RYT 121 6208/1	TBGA 400	1
	Heat sink for BCM5680		SEA 103 25		1
	10/100/1000Mbit Quad PHY	BCM5404KBT / Broadcom	RYT 121 6209/1	TBGA 268	2
	PCI bridge 40 MHz	QSpan II / Tundra	RYT 121 6200/1	PBGA 256	1
	QBus arbiter (PLD)	EPM7032AE / Altera	RYT141 6017/C	TQFP44	1
	Oscillator 25 MHz ±50ppm		RTL 201 028/19		1
	Oscillator 140 MHz ±100ppm	VPC1-B1A-140M000 / Vite Technology Express	RTL 201 032/07		1
	PLL clock driver	CY2309ZC-1H / Cypress	RYT 109 6149/C		2
	Magnetic	Bel Fuse	REG 735 9205/1		8
	Front connector		RPV 431 1911		8

Table 23: Main components.

The table below shows the programmable component on GESB (the PLD and the Flash). They are in-system-programmable.

Component	Type /Vendor	Product number	Package]	Qty
PLD	EPM7032AE / Altera	RYT141 6017/C	TQFP44	1
Flash	RC28F320C3/ Intel	RYT 118 6152/4	EBGA64	2

Table 24: Programmable component.

6 MECHANICAL DESIGN

6.1 PCB

Board	TVJ 828 410	Comments
Size [mm]	265mm x 207,5mm (TVJ828)	Required
Thickness [mm]	2.16 mm	
Number of Layers	12	
Number of Signal -Layers	6	
Technology	See UAB 105 83-036	
Impedance	50 Ω controlled impedance	See below

Table 25: PCB Characteristics.

According to the application note for BCM5404 (see reference 21), the following impedance characteristics has been implemented:

- The TRDP and TRDN signal traces has been routed with characteristic single-ended impedance of 50 Ω each.
- The differential TRDP/TRDN connections from the BCM5404 to the connector, maintain constant 100 Ω differential impedance.
- The controlled impedance (with respect to VDD for signals between PHY and 1:1 transformer) is 50 Ω.
- The controlled impedance (with respect to chassis ground for signals between 1:1 transformer and connector) is 50 Ω.

6.2 PBA

The PBA is using the building practice known as the Module Packing System BYB 501+.
Surface mounted and hole mounted components are used. Components are assembled on the primary and secondary side.
The GESB has ESD areas.
Stiffener is not used.
Mechanical guidance and slot coding is used.
The spacing in sub rack needed for the GESB is 30mm.
Soldering process: Re-flow soldering on primary and secondary side.

6.3 HIERARCHICAL DESIGN

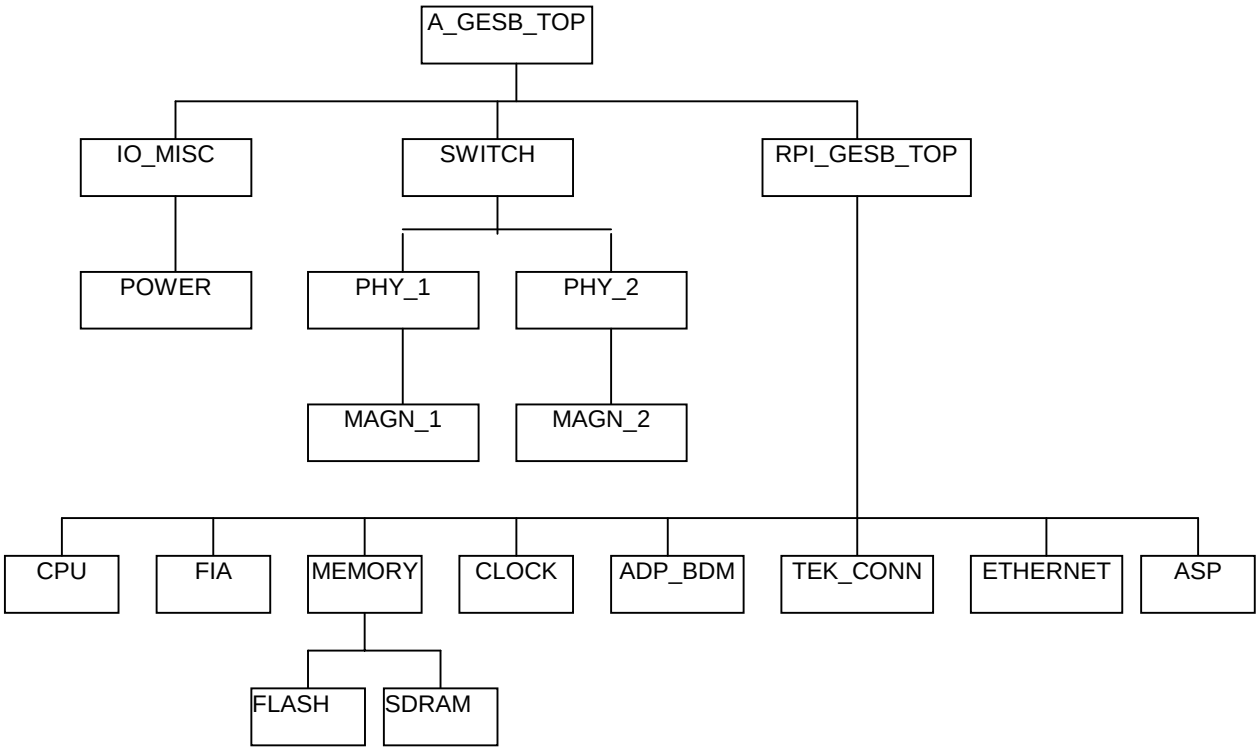

Figure 15: Hierarchical design.

GESB_TOP: include block-diagram.
IO_MISC: include back plane, front and Mbus.
SWITCH: include clock, BCM5680 and QSpan II.

6.4 FLOOR PLAN

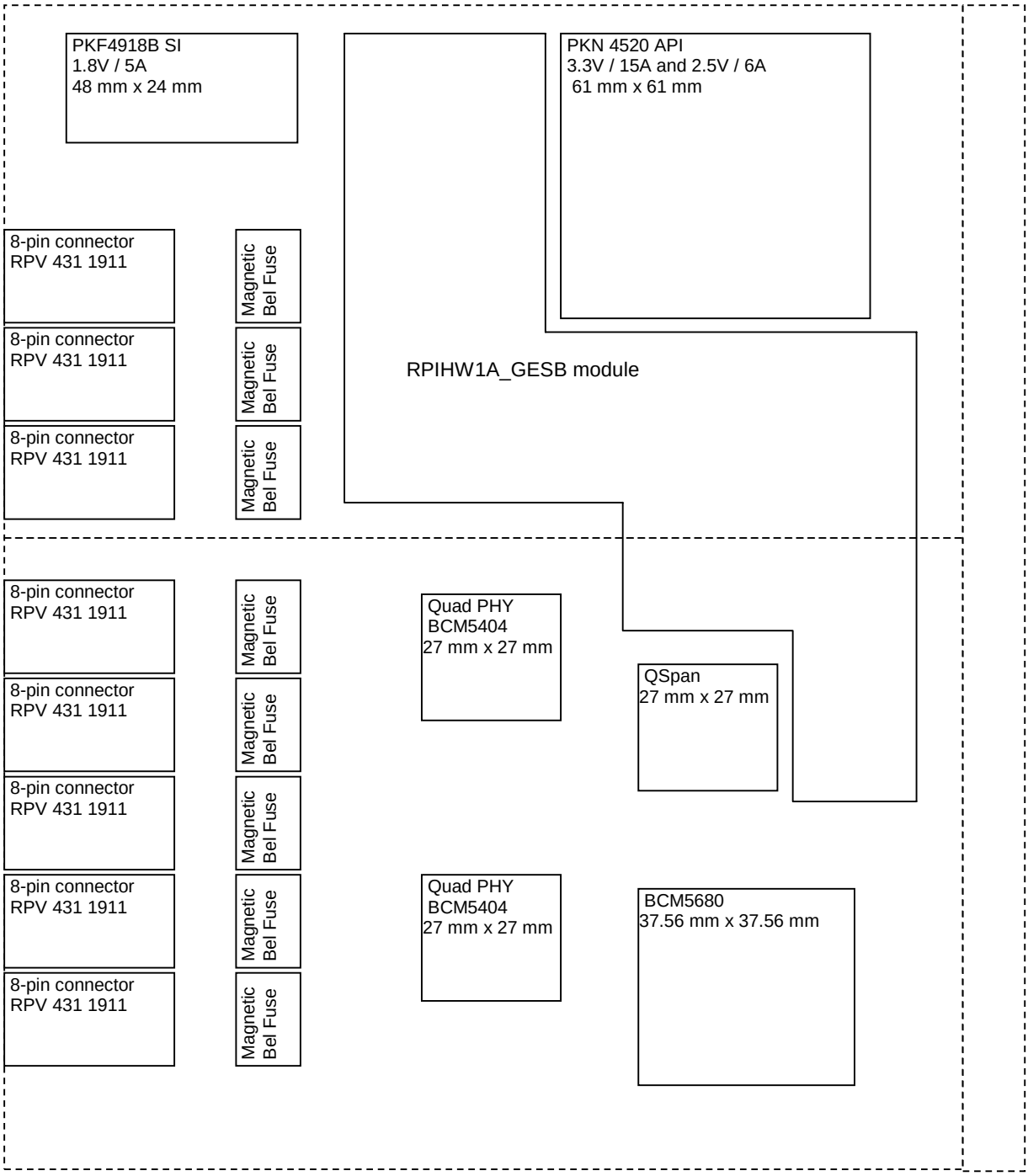

Figure 16: Floor plan.

6.5 CONNECTOR PIN ALLOCATION

6.5.1 Front connectors.

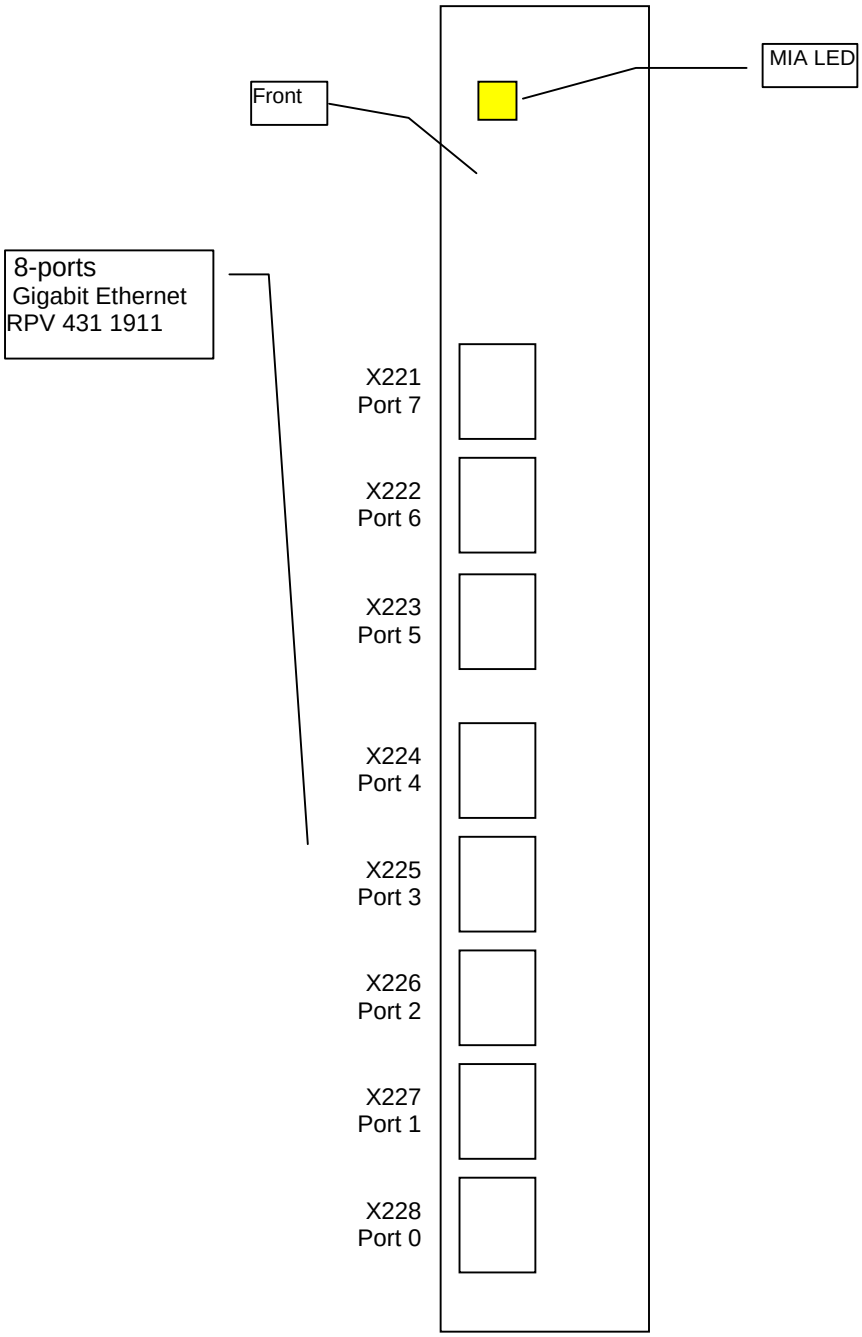

Figure 17: Front connector allocation.

ROW	COLUMN	
	A	B
1	TDN3	TDN0
2	TDP0	TDP3
3	TDP1	TDN2
4	TDP2	TDN1

Table 26: X101-X108, Gigabit Ethernet Port RPV 431 1911.

Connector	Port number
X221	7
X222	6
X223	5
X224	4
X225	3
X226	2
X227	1
X228	0

Table 27: X221-X228, Gigabit Ethernet Port RPV 431 1911.

Regarding port numbering see also chapter 2.2 and 4.4.

6.5.2 Back plane Connectors

All power is supplied through a two-blade power contact (4 pins/blade) one for each branch. The connectors are placed in the top of the magazine. Pin number 1-4 is always GND.

The connectors SXA2101008/1 are to be used.

Connector	Pin	
	1-4	5-8
XP01	GND	-48V_A
XP02	GND	-48V_B

Table 28: XP01 and XP02.

The new designed 5-row TERADYNE connector (wafer) is special made for two differential pairs/row and to fit the 15 mm PBA space.

Back plane connectors SXA2101005/1 are used.

ROW	COLUMN				
	A	B	C	D	E
01	SENSE_U	MB_WC	GND	JTAG2_TCK	JTAG2_TRST
02	MB_A0	MB_A1	GND	MB_A2	MB_A3
03	MB_A4	MB_SDA	GND	JTAG2_TDI	JTAG2_TMS
04	MB_SCL	MB_3V	GND	JTAG2_TDO	ASP_BYPZ
05	NC	NC	GND	NC	NC
06	NC	NC	GND	NC	NC
07	NC	NC	GND	NC	NC
08	NC	NC	GND	NC	NC
09	NC	NC	GND	NC	NC
10	NC	NC	GND	NC	NC

Table 29: X01 (Mbus address and JTAG2; Bscan ASP).

See reference 19, chapter 10.8.

ROW	COLUMN				
	A	B	C	D	E
01	10BaseTA_TXP	10BaseTA_TXN	GND	10BaseTB_TXN	10BaseTB_TXP
02	10BaseTA_RXP	10BaseTA_RXN	GND	10BaseTB_RXN	10BaseTB_RXP
03	NC	NC	GND	NC	NC
04	NC	NC	GND	NC	NC
05	NC	EA_SRE	GND	EB_SRE	AP_0-SP
06	AP_0-S0	AP_0-S1	GND	AP_0-S2	AP_0-S3
07	NC	NC	*GND*	NC	NC
08	NC	NC	*GND*	NC	NC
09	NC	RPB_MA_TX	GND	RPB_MB_TX	NC
10	NC	RPB_MA_RX	GND	RPB_MB_RX	NC

Table 30: X10 (Ethernet 10Base-T, Magazine address taken from AP-0 and RPB-S).

See reference 19, chapter 10.15.

ROW	COLUMN				
	A	B	C	D	E
01	AP_1-S0	AP_1-S1	GND	AP_1-S2	AP_1-S3
02	AP_1-SP	AP_3-S0	GND	AP_3-S1	AP_3-S2
03	AP_3-S3	AP_3-SP	GND	BADR-S0	BADR-S1
04	BADR-S2	BADR-S3	GND	BADR-S4	BADR-SP
05	MTC_TRSTZ	JTAG1_TCK	GND	JTAG1_TDI	MTC_TDO
06	JTAG1_TRSTZ	JTAG1_TMS	GND	JTAG1_TDO	FWZ
07	TAP_HRSTZ	TRG	GND	FWPEZ	NC
08	P3V	PGND	GND	TMPZ0	TMPZ1
09	MTC_TCK	V24_TX	GND	V24_RX	NC
10	SENSE_L	MTC_TMS	GND	MTC_TDI	Vcc_mon

Table 31: X11 (Sub rack address taken from AP-1, Sub rack address taken from AP-3, Board address, hard-coded in the back plane, MTC FIA and JTAG1)

See reference 19, chapter 10.16.

6.5.3 Test connectors

Pin	Signal	Pin	Signal
1	VFLS0	2	BDM_SRSTZ
3	GND	4	DSCK
5	GND	6	VFLS1
7	HRESETZ	8	DSDI
9	+3,3V	10	DSDO

Table 32: BDM connector.

Pin	Signal	Pin	Signal
1	RXD2	2	PB30_S0
3	TXD2	4	PB30_S1
5	RXD1	6	PB29_S2
7	RXD2	8	N.C.
9	N.C.	10	ADP_SRSTZ
11	GND	12	ADP_HRSTZ
13	N.C.	14	LED1
15	N.C.	16	LED2
17	N.C.	18	LED3
19	N.C.	20	N.C.

Table 33: ADP connector.

7 VERIFICATION AND TEST

7.1 BOUNDARY SCAN CHAIN ON THE GESB

The GESB contains 7 components (including the 2 components in the RPIHW1A_GESB module: MPC860P and FIA) supporting boundary scan according to JTAG standard IEEE 1149.1. The ASP functionality connects the JTAG chain (RPI part and the rest of the board).
The BCM5680 tests all the internal memory and tables at power up.
The boundary scan chain on GESB is shown in the following figure.

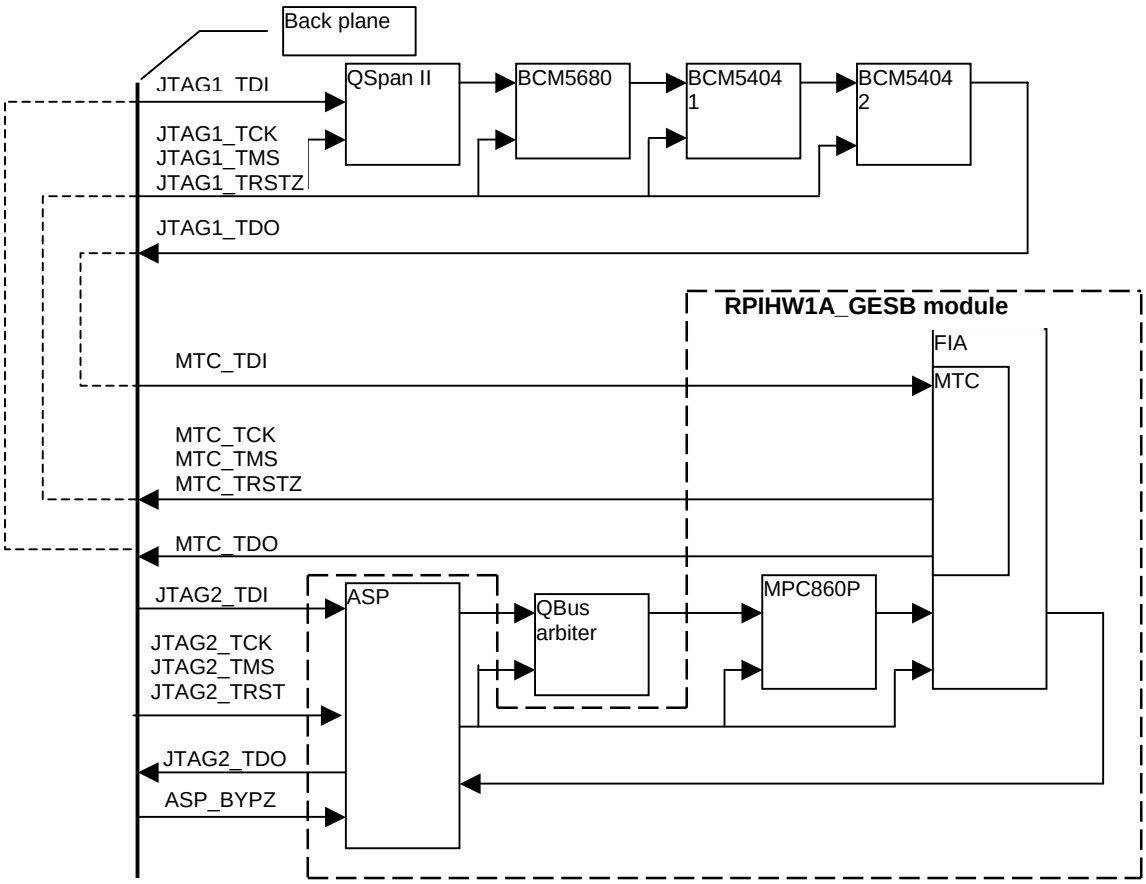

Figure 18: Boundary Scan Chain of the GESB.

The simplified figure above shows the signal flow of the test data signal and the remaining signals (TRSTZ, TMS, and TCLK).

7.2 DESIGN FOR BASIC TEST

The GESB includes the following features to support the verification process during Basic Test:

- BDM interface. For debugging and testing of the MPC with help of an emulator.
- ADP interface. For debugging and testing of the MPC with help of the RP Tool Box.
- MPC-bus test connectors. These connectors allow the observation of the processor bus by connecting a logic analyser to the test connectors.
- PCI-bus test connectors. These connectors allow the observation of the PCI bus (data/address and control signals).
- QBus arbiter test connector.
- MDIO and MDC signals on test connector.
- Two indications LED's for each port.

Note: All the mentioned test connectors and LED's will not be mounted on the final product.

7.3 DESIGN FOR PRODUCTION TEST

The GESB provides Boundary Scan functionality for production test.
The GESB is prepared to support P-BIST via the back plane.

8 ENVIRONMENTAL REQUIREMENTS

8.1 RELIABILITY

The mean time to failure (MTTF) at 25°C ambient temperature is at least 78 years on the GESB.

8.2 TEMPERATURE

According to reference 18, the GESB fulfils the following temperature ranges:

Normal operation:	+ 5°C ... +40°C
Safe operation:	- 5°C … +50°C
Non destruction:	-10°C ... +55°C

8.3 EMC

The GESB complies with requirements stated in reference 11.

8.4 ESD

The GESB complies with requirements stated in reference 11.

9 ABBREVIATION

Abbreviation	Explanation
ADB	Application Device Bus
ADP	Advanced Debug Port
ASIC	Application Specific Integrated Circuit
BDM	Background Debug Mode interface
BGA	Ball Grid Array
BIST	Built In Self Test
BYB 501	An Ericsson standard of equipment practice
CP	Central Processor in AXE-10 terminology.
CPU	Central Processing Unit
DL34	Digital Link adaptable from version 3 to 4
DMA	Direct Memory Access
DRAM	Dynamic Random-Access Memory
EMC	Electro Magnetic Compatibility
ESD	ElectroStatic Discharge
Ethernet	Local Area Network IEEE 802.3
FIA	A MPC860 support ASIC developed at UAB
GEM	Generic Ericsson Magazine
I^2C	Inter-IC bus.
IEC	International Electro-technical Commission
IEEE	Institute of Electrical and Electronics Engineers
IP	Implementation Proposal or Internet Protocol
JTAG	Joint Test Action Group, IEEE 1149.1
LED	Light Emitting Diode
MAC	Media Access Control
MIA	Manual Intervention Allowed
MDI	Media Dependent Interface (Ethernet)
MII	Media Independent Interface (Ethernet)
MTC	Master Test Controller
MTTF	Mean Time To Failure
NSP	Network Server Platform
O&M	Operation and Maintenance
PBA	Printed Board Assembly, a PCB with mounted components.
P-BIST	Processor Controlled Built In Self Test
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PHY	Physical Interface circuit (for Ethernet)
PLD	Programmable Logic Device
PLL	Phase Locked Loop
PQFP	Plastic Quad Flat Pack
RFC	Request for comments
RMON	Remote Monitoring
RNS	Radio Network Server
RP	Regional Processor

RPB	Regional Processor Bus
RPB-S	Serial RP Bus
RPI	Regional Processor Integrated (hardware module)
SCC	Serial Communication Controller
SCB-RP	Support and connection board with an RP
SDRAM	Synchronous DRAM
SMC	Serial Management Controller
TAP	Test Access Port
TCP	Transmission Control Protocol
Telnet	Remote Access Protocol
TSP	TSP Server Platform
UART	Universal Asynchronous Receiver Transmitter
V.24	ITU-T standard for serial communication. Similar to the IEC standard RS-232.
VLAN	Virtual Local Area Network

10 REFERENCES

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