

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.	
UABGLS		102 62 - BFD 508002/1 Uen	
Dokansv/Godkänd - Doc respons/Approved	Kontr - Checked	Datum - Date	Rev
UAB/H/MMC (Anders Stenkvisst)		2001-12-13	D

GENERIC ERICSSON MAGAZINE (GEM)

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(1) Revision Information

Revision	Date	Comment
A	2000-05-30	GEM designed for SCB-RP with 8row connector
B	2000-06-27	GEM designed for SCB-RPB with two times 5row connectors Magazine code key removed Minor updates in the document
C	2001-06-20	Maintenance bus for AP_0 included New pinout for AP_2 CGB delay changed
D	2001-12-13	General: Insulation (clearances) improved between -48V and 0V Voltage supervision input changed from connector X01 to XP07-XP10 (SCB position).

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1 GENERAL

This Design Specification describes the hardware design of the new Generic Ericsson Magazine GEM.

1.1 PURPOSE

The document shall cover the implementation, be the base for the design and represent the main input. The document will also include some general information regarding PBAs in GEM.

1.1.1 Introduction

The magazine is developed for full size PBA ROJ208 = PCB TVJ 828 designed in the ARIADNE (APT 1.5) project.

2 REQUIREMENTS ON CHARACTERISTICS

See reference Table 1.

3 REFERENCES

Table 1. References

Document No.	Rev.	Title	Ref. No.
19/15941- FCP 105 1003 Uen	B	Implementation Proposal for a Generic AXE Magazine GEM	[1]
102 62 ROJ 208 323/1 Uen	B	Design Specification for the SCB-RP HW	[2]
102 62 ROJ 207 123/1 Uen	A	Design Specification for the MEP HW	[3]
15/15941- FCP 105 1003 Uen	A	Clock & NS HW in Beamon	[4]
14/15941- FCP 105 1003 Uen	A	Beamon DLMUX Implementation Proposal	[5]
13/15941- FCP 105 1003 Uen	A	Implementation Proposal for the switch core in Beamon	[6]
1/15941-FCP 1051007/F Uen	A	Implementation Proposal ET155-1 HW	[7]
1520-FDB 11 02 Uen	A	P-BIST design for testability rules	[8]
2/0363-FCP 105 1003 Uen	A	Clock Workshop Technical Report	[9]
8/15519-ANT 213 18/1	A	Specification of DL34 Interface	[10]
1056-BYT 10102	A	General requirements for telecom equipment practice and its properties	[11]
U 93 0330	D	EMC requirements for AXE	[12]
UAB/O-96:096	A	Identity for Hardware Products in AXE-10	[13]

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Document No.	Rev.	Title	Ref. No.
4/155 19-APZ 212 20	A	Maintenance Bus, MB	[14]
UAB/B/R-96:033 Uen	PE1	RPS backplane and cable interfaces for HWM products	[15]

4

ABBREVIATIONS

The table below lists of the abbreviations and terminology used in this paper

Table 2. Abbreviations.

Abbreviation	Explanation
AP	Address Plug
ASP	Addressable Scan Port
BIST	Built In Self Test
CDB	Clock Distribution Board
CDM	Clock Distribution Magazine
CGB	Clock Generation Board
CLK	Clock
CLK_CD	Clock from CGB Distribution
CLK_CX	Clock CLM to Core
CLM	CLock Module
CSPB	Common Speech Processing Board
DEV	DEvice board (shall not be connected with DEV for channel)
DL3	Digital Link variant 3, with 16 DL2 channels.
DL34	Digital Link version 4
DL5	Digital Link version 5
DLEB	Digital Link multiplexer for Existing equipment Board
Ethernet	Local Area Network IEEE 802.3
FIA	A MPC860 support ASIC developed at UAB
GEM	Generic Ericsson Magazine
GDM	Generic Device Magazine
I ² C	Two-wire serial multi-master bus used in the M-bus.
IRB	Incoming Reference Board
ISP	In-System-Programming
JTAG	Joint Test Action Group, IEEE 1149.1
LED	Light Emitting Diode
MB	Maintenance Bus
MIA	Manual Intervention Acknowledged
MTC	Master Test Controller

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Abbreviation	Explanation
NNRP	Network Node Renewal Process
P-BIST	Processor controlled, PROM based, built-in self test.
PBA	Printed Board Assembly, a PCB with mounted components.
PCB	Printed Circuit Board
PIU	Plug In Unit. Consist of one or more PBAs.
PSI	Protection Switch Interface
QUICC	QUad Integrated Communication Controller
RP	Regional Processor
RPB-S	Serial RP Bus
RPB/I.	RPBus Incoming, to and from CP.
RPB/O.	RPBus Outgoing, to and from next RP.
RPB/M.	RPBus Magazine internal, to and from one path in backplane.
RPB/M-A.	RPBus Magazine internal, path A.
RPB/M-B.	RPBus Magazine internal, path B.
SCB-RP	Support and Control Board - with an RP
SYNC_CX	SYNChronization link from CLM to core
SYNC_XC	SYNChronization link from core to CLM
TAP	Test Access Port
TSHOD	Two Stage High Ohmic Distribution
V.24	ITU-T standard for serial communication. Similar to the IEC standard RS-232.
XDB	Distributed Switch Board
XNB	Switch Board for Network Node Renewal Process (NNRP)
1000Base-T	1Gbit/s ethernet for cable

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5 FUNCTIONAL DESCRIPTION

In GEM following main interfaces will be interconnected:

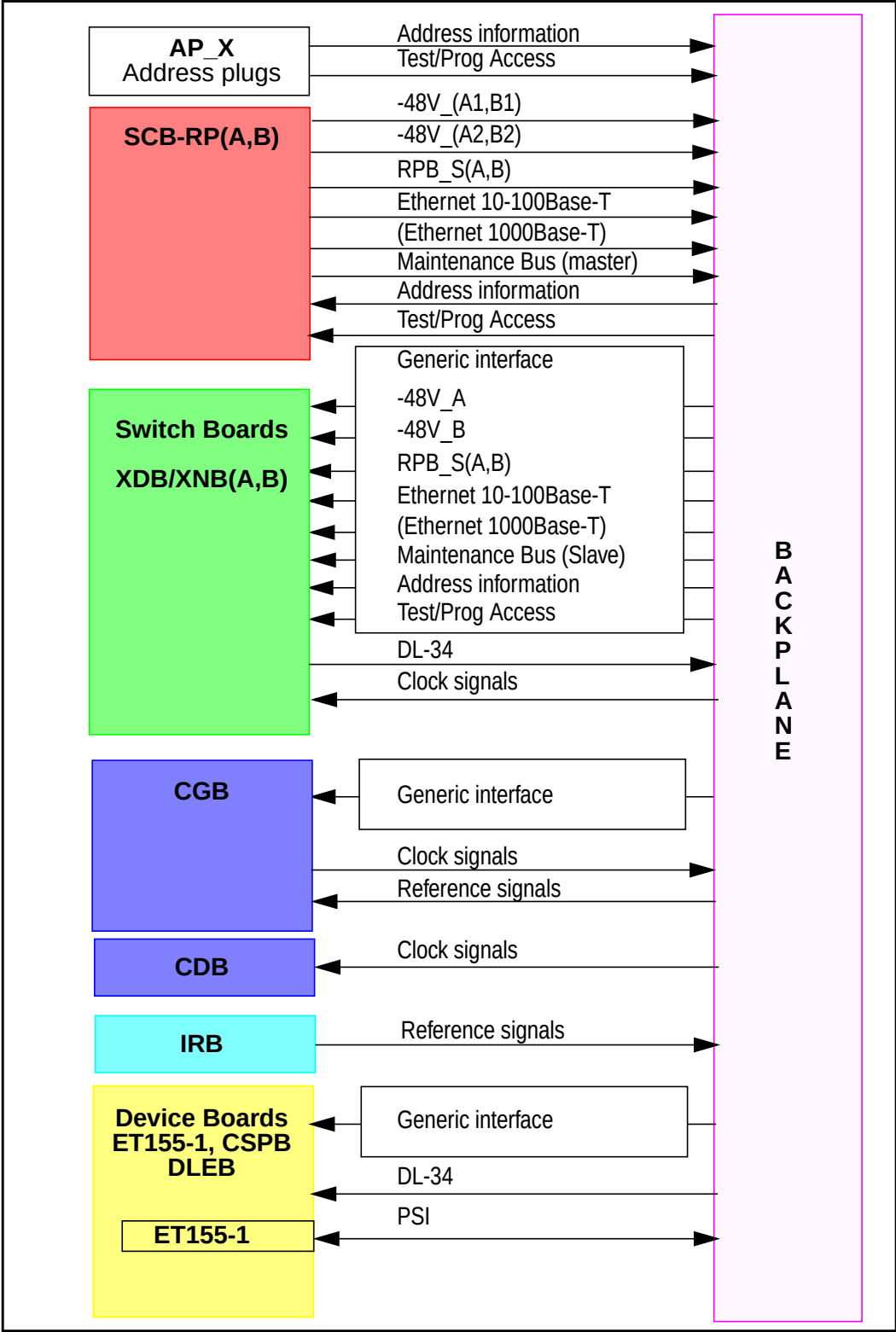


Fig.1. GEM interface

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.		102 62 - BFD 508002/1 Uen
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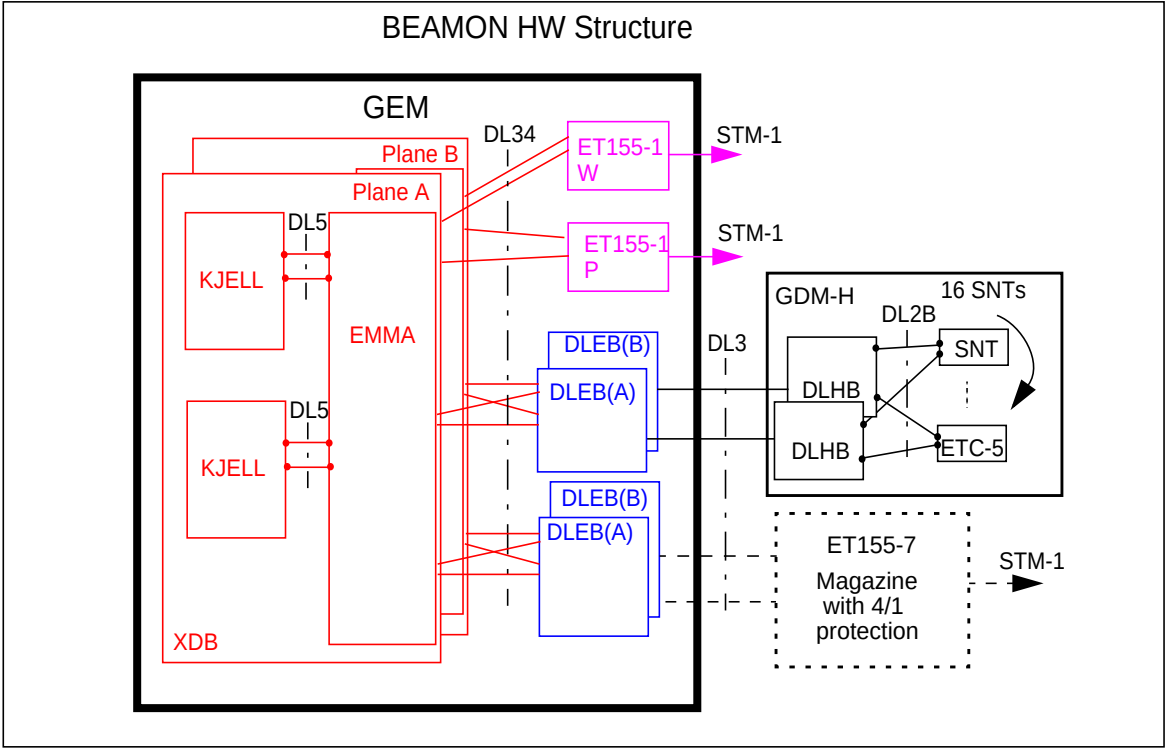


Fig.2. XDB interface

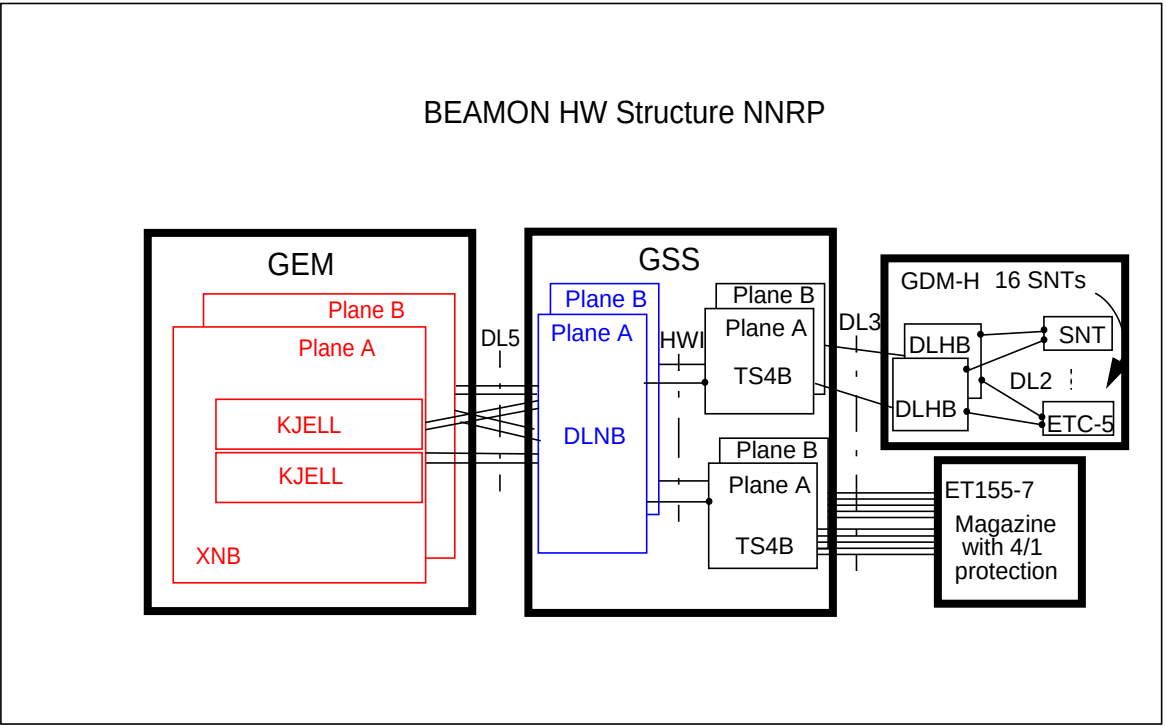


Fig.3. XNB interface

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PBA POSITIONS IN GEM**Table 3. Mixing possibilities**

Acronym				BOARD COMBINATIONS		
Physical_Pos	mm	Board_ADR	DEV pos			
X02	0	0		SCB-RP_A_M SCB-RP_A_D		
X05	15					
X08	30	1	DEV 0	XDB_A		
X11	45	2	DEV 1	ET155-1, CSPB , DLEB	XNB_A_0	
X14	60	3	DEV 2	ET155-1, CSPB , DLEB		
X17	75	4	DEV 3	ET155-1, CSPB , DLEB		
X20	90	5	DEV 4	ET155-1, CSPB , DLEB	XNB_A_1	
X23	105	6	DEV 5	ET155-1, CSPB , DLEB		
X26	120	7	DEV 6	ET155-1, CSPB , DLEB		
X29	135	8	DEV 7	ET155-1, CSPB , DLEB	XNB_A_2	
X32	150	9	DEV 8	ET155-1, CSPB , DLEB		
X35	165	10	DEV 9	ET155-1, CSPB , DLEB	IRB	
X38	180	11	DEV 10	ET155-1, CSPB , DLEB	CGB_X	
X41	195	12	DEV 11	ET155-1, CSPB , DLEB		
X44	210	13	DEV 12	ET155-1, CSPB , DLEB	XNB_B_0	
X47	225	14	DEV 13	ET155-1, CSPB , DLEB		
X50	240	15	DEV 14	ET155-1, CSPB , DLEB		
X53	255	16	DEV 15	ET155-1, CSPB , DLEB	XNB_B_1	
X56	270	17	DEV 16	ET155-1, CSPB , DLEB		
X59	285	18	DEV 17	ET155-1, CSPB , DLEB		
X62	300	19	DEV 18	ET155-1, CSPB , DLEB	XNB_B_2	
X65	315	20	DEV 19	ET155-1, CSPB , DLEB		
X68	330	21	DEV 20	ET155-1, CSPB , DLEB	IRB	
X71	345	22	DEV 21	ET155-1, CSPB , DLEB	CGB_1	CDB_0
X74	360	23	DEV 22	ET155-1, CSPB , DLEB		CDB_1
X77	375	24	DEV 23	XDB_B		
X80	390	25		SCB-RP_B_M SCB-RP_B_D		
X83						

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7 MECHANIC

The mechanic follows the BYB501 specification.
Backplane stiffener shall be used for GEM.

7.1 SUBRACK DIMENSIONS

Subrack BFD 508 = (plug-in unit size Hs3=265 mm Ds0=225 mm).

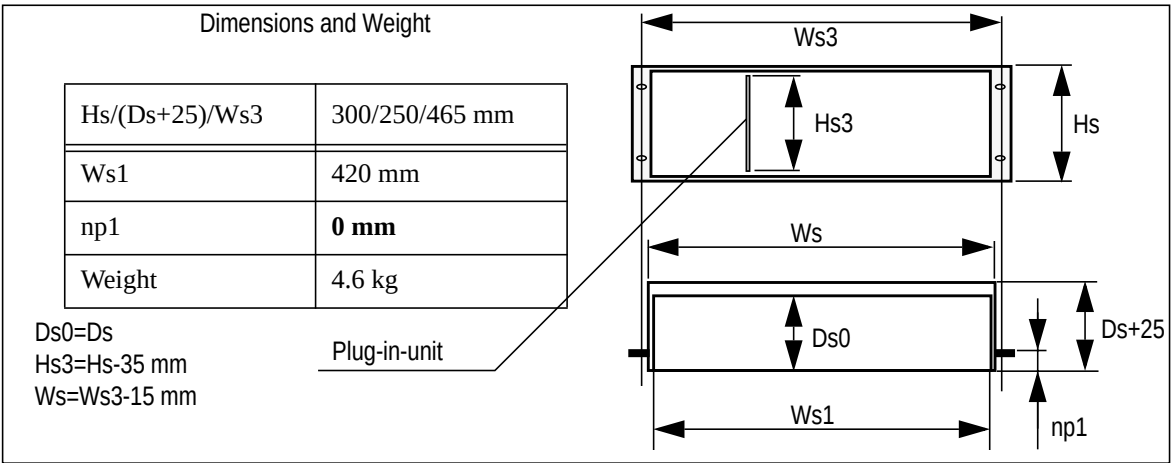


Fig.4. Subrack Dimensions

7.2 BACK-PLANE DIMENSIONS

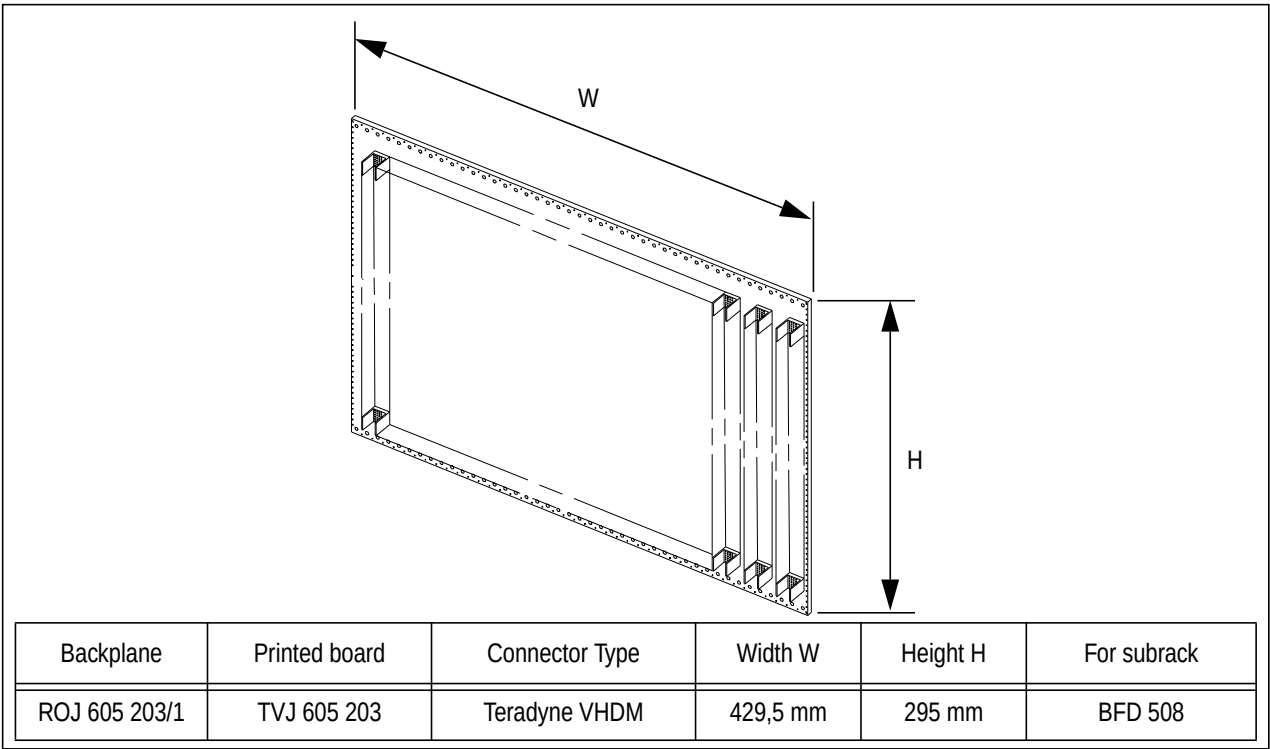


Fig.5. Back-plane Dimensions

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7.2.1 Layer information data

GEM will be designed with following data.

No of layers : 10

Pattern Class : 55

Layer specification : BYC101346

Layer drawing : 105 83-132

Table 4. Layer structure

Layer Primary side=1	Use	Pattern classes			Film	Viahole dia 0,5 mm 0 = No Hole 1 = Hole
		Conductor	Conductor insulation	Land		
1	Ground	52	54	54	Pos	1
2	Signal	55	55	54	Pos	1
3	Signal	55	55	54	Pos	1
4	Ground	52	54	54	Neg	1
5	Signal	55	55	54	Pos	1
6	Signal	55	55	54	Pos	1
7	Ground	52	54	54	Neg	1
8	Signal	55	55	54	Pos	1
9	Signal	55	55	54	Pos	1
10	Ground	52	54	54	Pos	1

ENGINEERING DATA LAYER 2, 3, 5, 6, 8 AND 9

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7.3 PBA DIMENSIONS

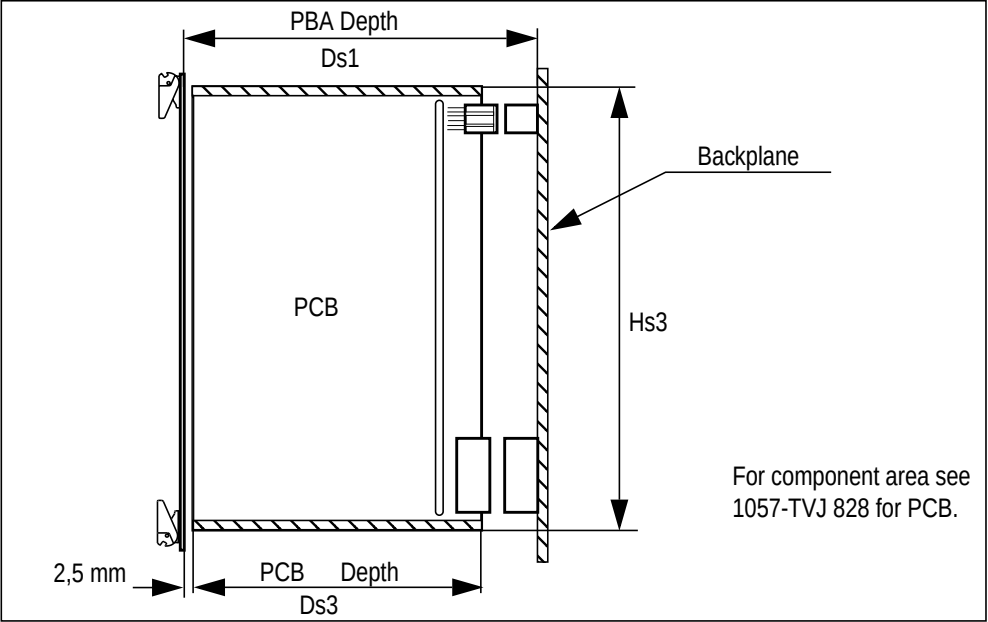


Fig.6. PBA size

Table 5. PBA data

Function	PBA	Hs3	Ds1	PCB	Ds3	Connector Type
All PBAs	ROJ 208	265	225	TVJ 828	207,5	SXA 210 01 - 08/1 SXA 210 13 - 17/1

7.4 BACK-PLANE AND PBA CONNECTORS

Very High Density Metric connectors (VHDM) from Teradyne shall be used for backplane and PBAs.

To fit the 15mm PBA space the new 5-row connector shall be used for all boards.

Technical data.
Current rating: Signal contact 1* Amp at 70 degrees C
Current rating: Power contact 10* Amps at 70 degrees C

The maximum number of signal connectors for one PIU are 11 (440pins).

The number of used connectors vary for different positions.

* = Teradyne ratings

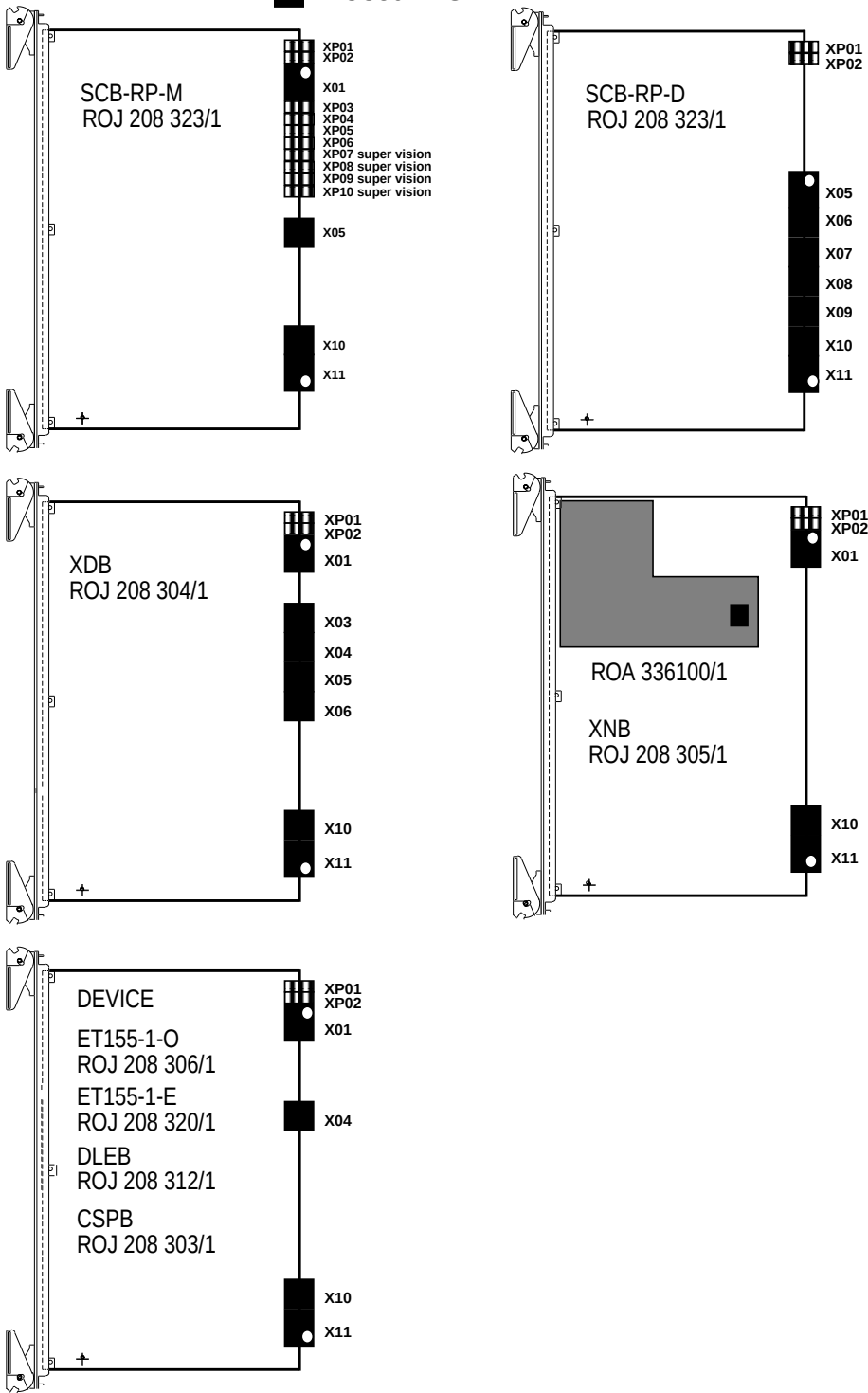
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7.5 CONNECTOR CONFIGURATIONS

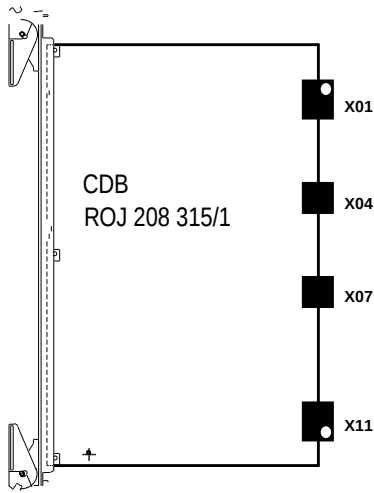
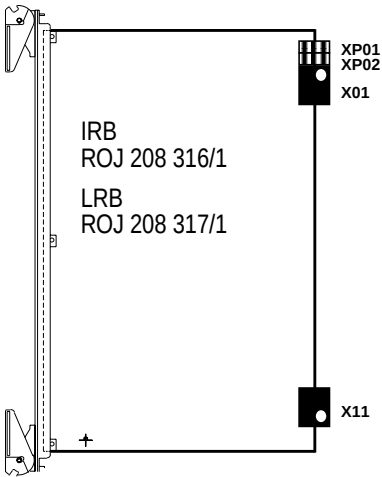
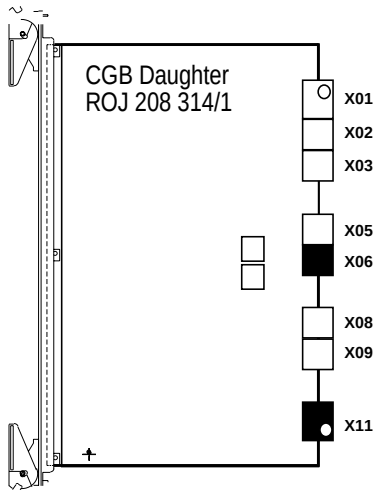
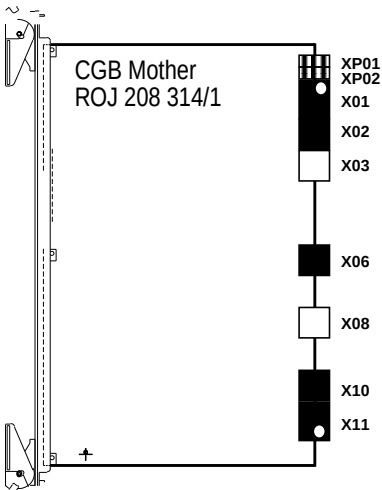
For a PBA the rear connectors will be assembled to one unit before mounting.
Following configuration are defined.

The RNV component shall be placed on the circuit diagram for the board with
item number X100 (graphic symbol).

■ = Used in GEM



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7.6 CODE KEYS FOR PLUG-IN UNITS

Code keys will not be used in GEM.

If code keys must be introduced standard keys from Teradyne shall be used.

7.7 PHYSICAL POSITION

Horizontal physical position for a plug in unit is defined as the number of 5 mm steps from the inner left side of the subrack to the right side of the plug-in unit printed board. A 5 mm filling is used in the left side of the subrack, which result in physical position 2 for the first plug-in unit. Vertical physical position for a plug in unit is defined as the number of 5 mm steps from the external bottom side of the subrack to the bottom side of the plug-in unit printed board.

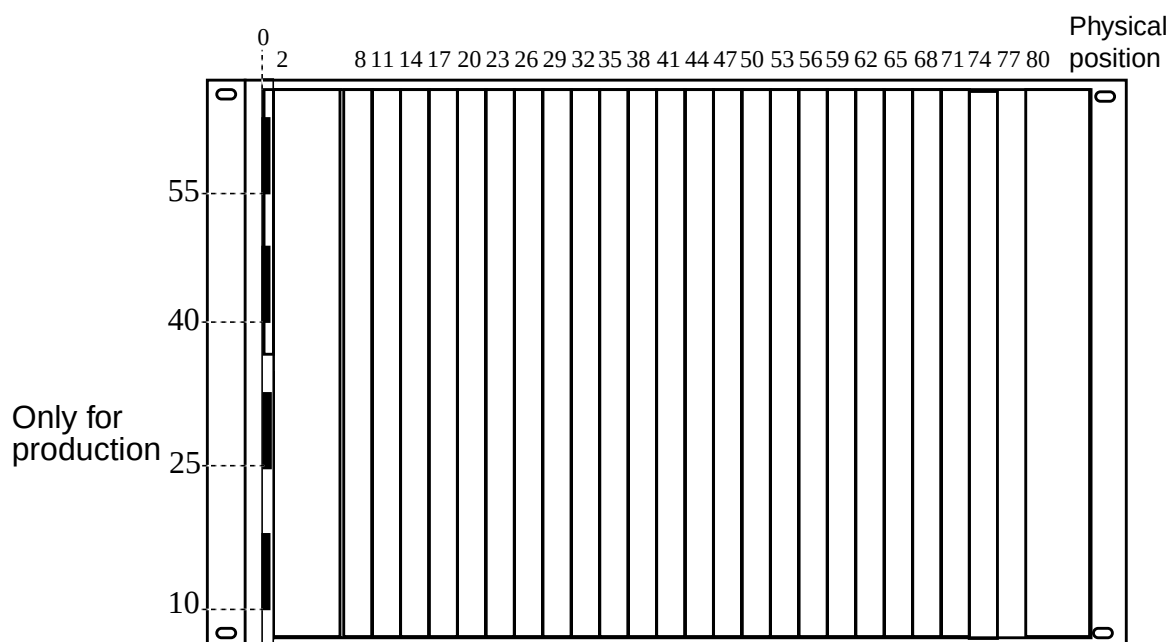


Fig.7. Physical position

8 INTERWORK

Following interfaces are available in GEM:

- -48 V, branch A1,A2 and B1,B2, supplied from SCB-RP
- Two dedicated short pins are used for hot plug in handling
- RPB-S, branch A and B, supplied from SCB-RP
- DL34, branch A and B, supplied from XDB
- PSI (Protecting Switch Interface between ET155-1 W/P)
- Ethernet, branch A and B, supplied from SCB-RP
- Internal and external clock distribution supplied from CGB

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- Incoming reference signals supplied from IRB
- Maintenance bus, supplied from SCB-RP
- MB address
- Board address, identification of board position
- Magazine address
- Address information for GSS/CLM purpose
- TAP
- MTC
- ASP bus (Addressable Scan Port)

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8.1 GEM VARIANTS

The figures below shows possible variants. Front connectors are only showed for switch boards.

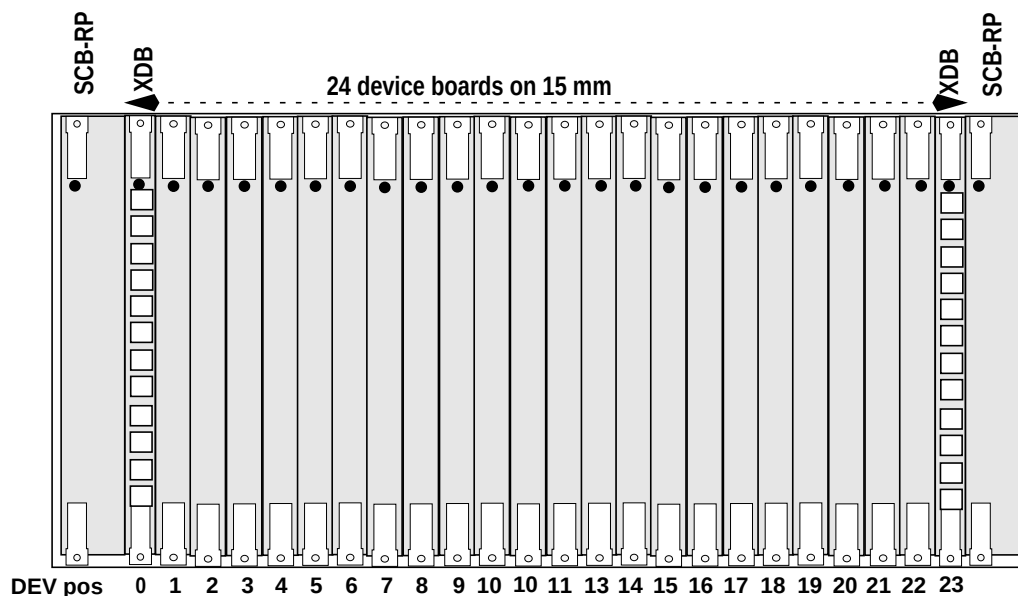


Fig.8. GEM

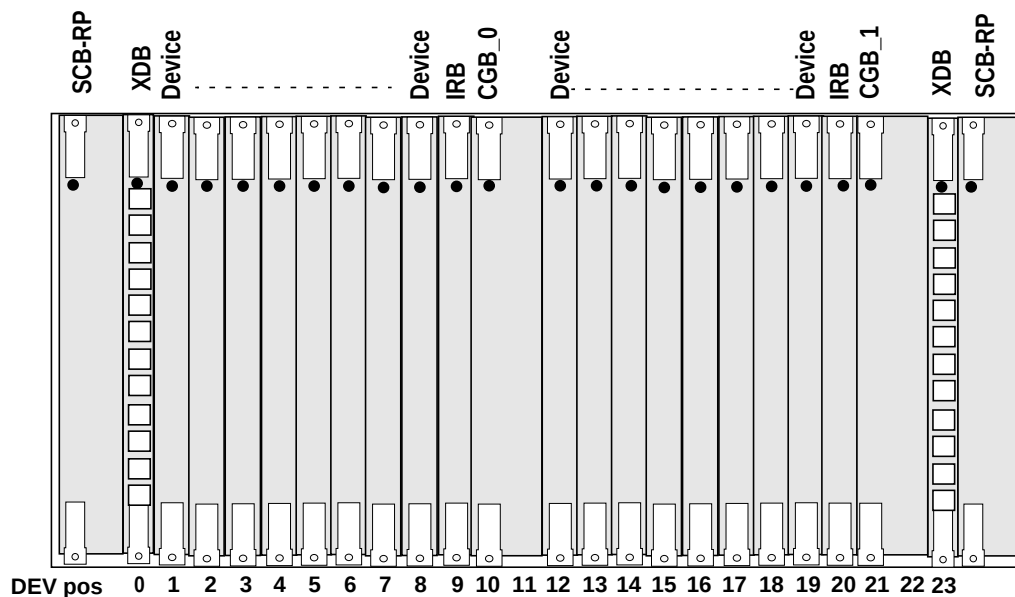


Fig.9. Single GEM solution $\leq 16K$

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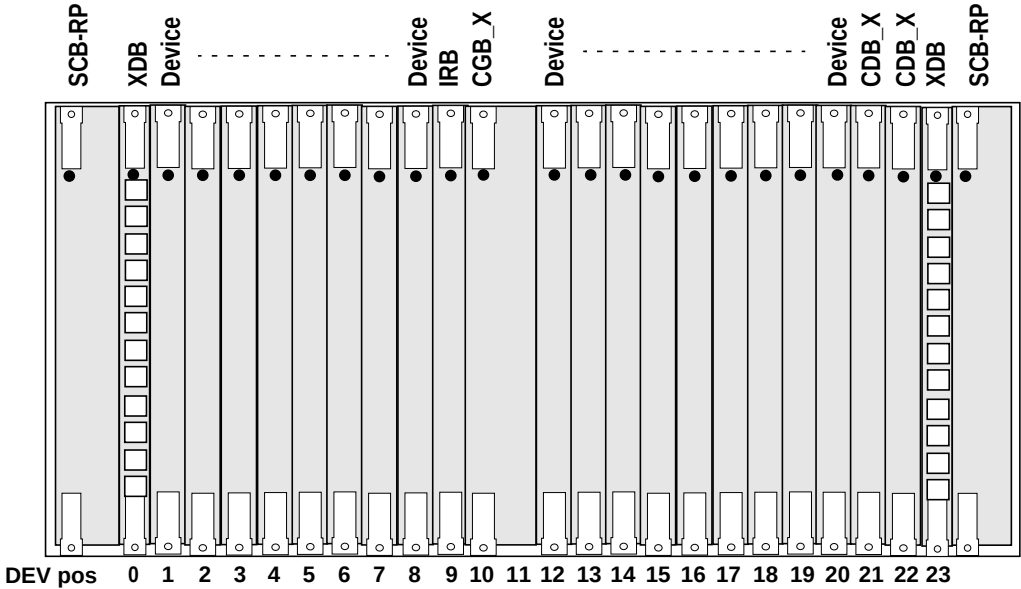


Fig.10. GEM with external clock distribution (max. 8 GEM)

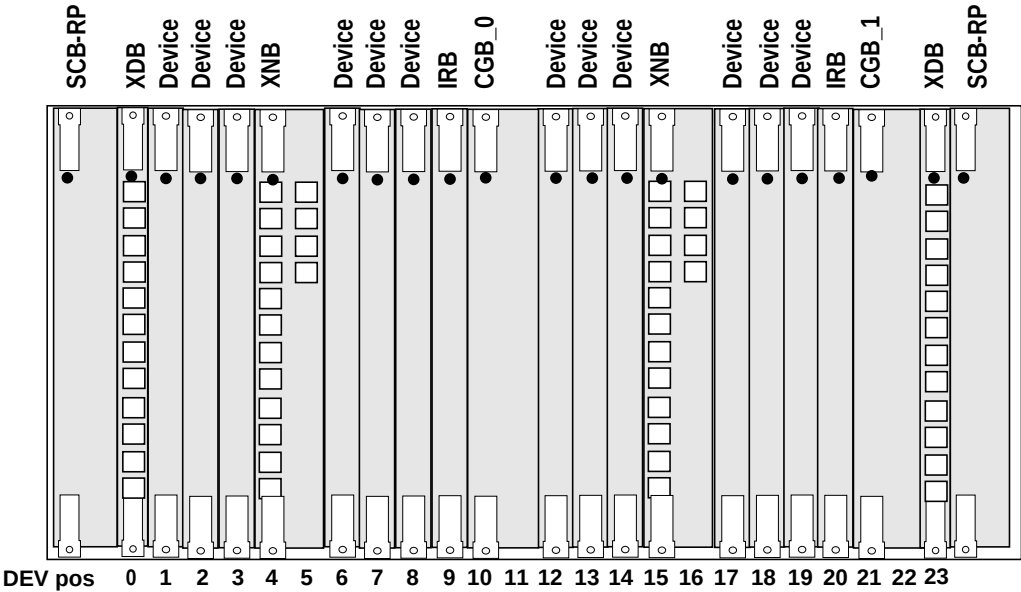


Fig.11. MixedGEM, XDB + 16K NNRP.

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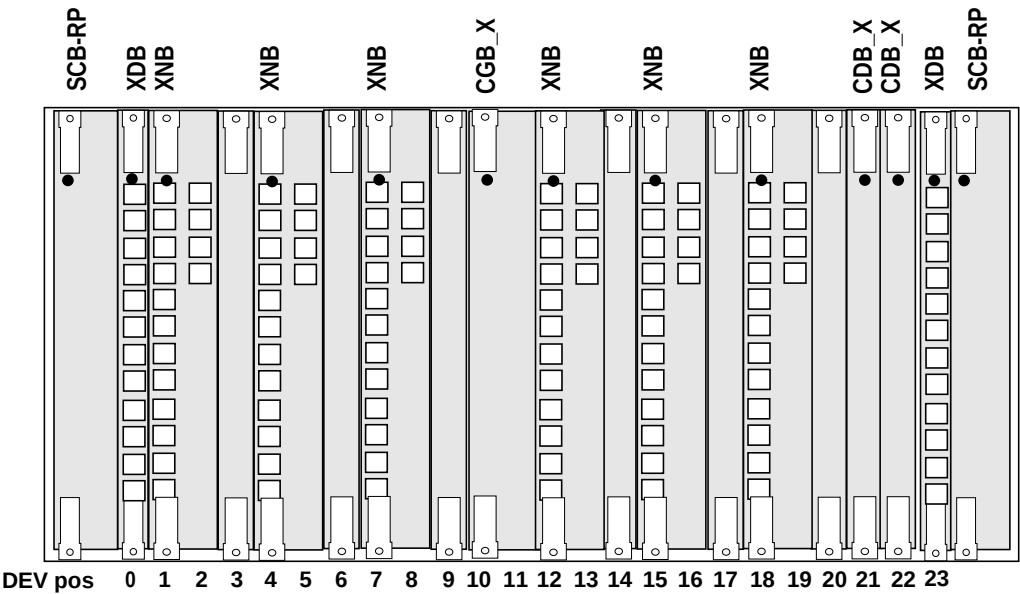


Fig.12. Pure NNRP 48K (Only 32K will be introduced)

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8.1.1 Clock Distribution Magazine

For equipment with more then eight GEM magazine a clock distribution magazine must be used (CDM).

9 PIN OUT DESCRIPTION

Following chapters describes the interface and the pin-out for all backplane signals

9.1 POWER DISTRIBUTION

9.1.1 Power Supply

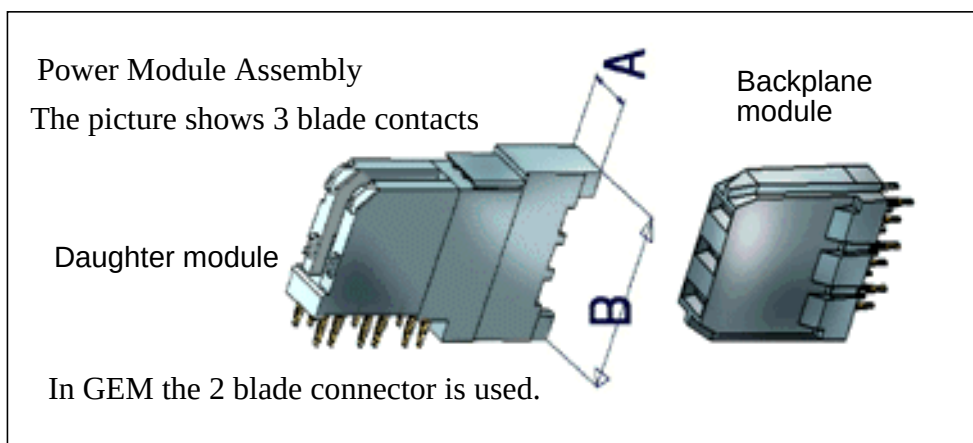
The SCB-RP board takes in -48V via two front connectors. The -48V is filtered and fed to the backplane in order to be distributed to all boards in the magazine via XP03, XP04 and XP05,XP06. XP07- XP10 are used for voltage super vision.

The magazine is divided in a left and a right half. The maximum power provided for each half is 400 Watts limited by the TSHOD distribution.

Since there exist two SCB-RP boards in a GEM the power supply is conveyed in two separate paths to each board.

Power Supply pin-out

Each blade is connected with four pins towards the backplane.



From each 400W filter the power is distributed via two power connectors (totally 4). The connectors XP03-XP06 are placed in the position for X02.

Pin number 1-4 are always GND.

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Table 6. SCB-RP XP03 - XP08

Acronym	Full name	Connector	Pin
GND	GND	XP03	1,2,3,4
-48V	-48V_A1(B1)	XP03	5,6,7,8
GND	GND	XP04	1,2,3,4
-48V	-48V_A1(B1)	XP04	5,6,7,8
GND	GND	XP05	1,2,3,4
-48V	-48V_A2(B2)	XP05	5,6,7,8
GND	GND	XP06	1,2,3,4
-48V	-48V_A2(B2)	XP06	5,6,7,8
GND	GND	XP07	1,2,3,4
-48V_A1	Super Vision A1	XP07	5,6,7,8
GND	GND	XP08	1,2,3,4
-48V_B1	Super Vision B1	XP08	5,6,7,8
GND	GND	XP09	1,2,3,4
-48V_A2	Super Vision A2	XP09	5,6,7,8
GND	GND	XP10	1,2,3,4
-48V_B2	Super Vision B2	XP10	5,6,7,8

Current rating: (10') Amps at 70 degrees C

* = Teradyne ratings

9.1.2

Power Users

The power input goes via two power connectors one for each branch.

The connectors are placed in the top of the magazine.

Pin number 1-4 are always GND.

Power User pin-out

Table 7. SCB-RP and DEV XP01, XP02

Acronym	Full name	Connector	Pin
GND	GND branch	XP01	1,2,3,4
-48V_A	-48V, branch A1(A2)	XP01	5,6,7,8
GND	GND, branch	XP02	1,2,3,4
-48V_B	-48V, branch B1(B2)	XP02	5,6,7,8

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2001-12-13

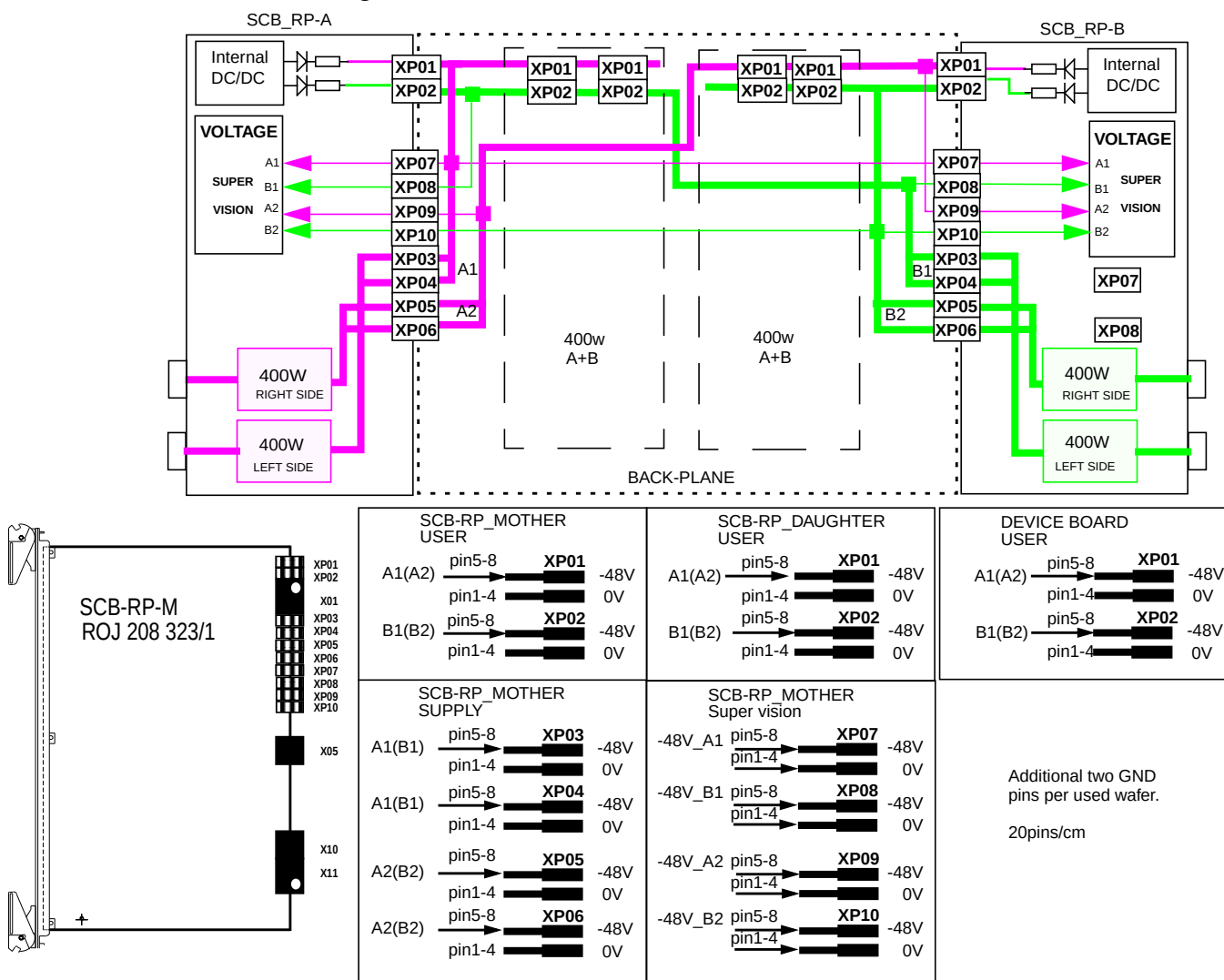
Rev

D

File

The -48V distribution is shown in the figure below

Fig.13. -48V distribution



Layout information

-48V branches shall be placed as a part of the signal and ground layers and dimensioned for a continuous current of 10A.

The power distribution shall be so low-ohmic that 50A transient at board insertion not shall cause any problem.

Recommendations:

The conductor width shall be chosen for 10A continuous current over the full life time. A long term current of 12A must not cause any fire hazards.

The maximum allowed resistance in the backplane -48V bus **conductor**, from inlet point to its furthest point shall be $\leq 35\text{mohm}$

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.		File
		102 62 - BFD 508002/1 Uen		
Dokansv/Godkänd - Doc respons/Approved	Kontr - Checked	Datum - Date	Rev	
		2001-12-13	D	

9.2 ADDRESS PLUGS

AP_0 will be used for RP address, AP_1 and AP_3 for Group Switch and CLM information. In production AP_2 will be used for boundary scan and flash programming.

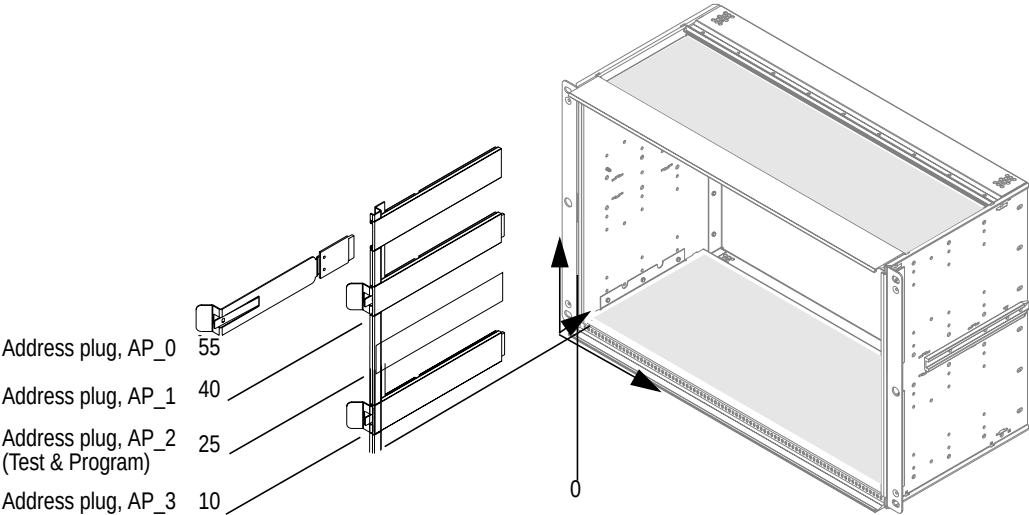
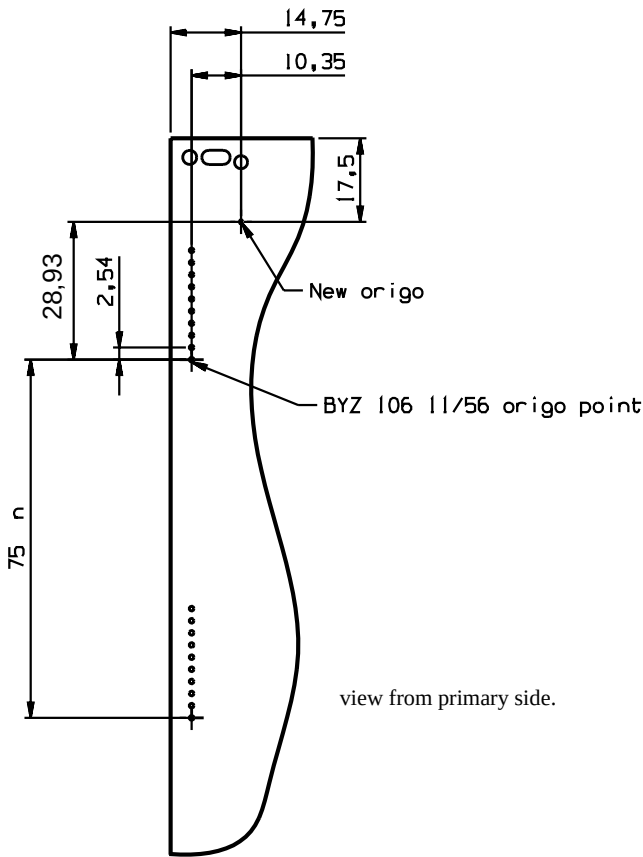


Fig.14. Address plugs

9.2.1 Address plug position



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Address Information

The address information is used to give a unique address or function.

- A RPI needs an physical RP address.
- A switch board needs to know where it is in the logical switch matrix, when the switch is built by more than one board.
- The clock function needs to know if it is CLM-0 or CLM-1.
- The maintenance bus needs a board address
(**board address is equal to slot number**).

9.2.2 RPI-block address

Address plug AP_0 (magazine address) is used for physical RP address and **available in all slots**. For protection all PBAs shall implement schottky diodes see figure 15 (RKZ 323 102/1).

The addresses are decoded from a combination of the board address (slot position) and the AP_0 value **by the RP**.

AP_0 also include signals for future use of magazine ID (green signals).

Table 8. Address information for RPI.

Acronym	Full name	Connector	Pin	AP_0 pin
AP_0-S0	RPADDR, bit 0	X10	A06	10
AP_0-S1	RPADDR, bit 1	X10	B06	9
AP_0-S2	RPADDR, bit 2	X10	D06	8
AP_0-S3	RPADDR, bit 3	X10	E06	7
AP_0-SP	Even parity S3-S0	X10	E05	6
GND	GND			5
MB_WC	MB_WC	X01	B01	4
SDA	MBA_SDA_1	X0201	D07	3
SCL	MBA_SCL_1	X0201	A07	2
3,3V	MBA_3V	X0201	D05, E05	1

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.		102 62 - BFD 508002/1 Uen	
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		2001-12-13		D	File

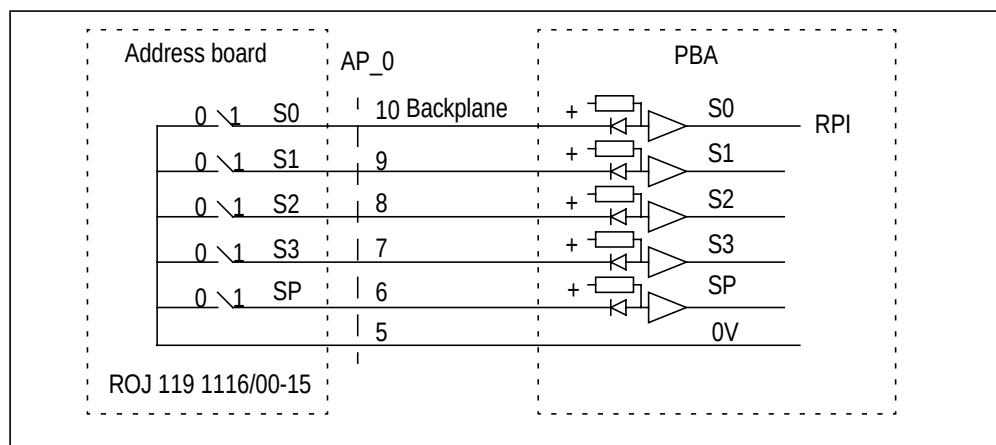


Fig.15. Magazine address implementation

9.2.3

GSS and CLM

Address plug AP_1 and AP_3 are used for switch matrix address and CGB board information, but will be **available in all slots**. PBAs using the address information shall implement schottky diodes (RKZ 323 102/1) see figure 16.

AP_1-S0 to -S2 indicate the magazine start address in a column and AP_3-S0 to AP_3-S1 indicate which row the magazine is placed in. In the parity bit check all bits shall be considered for each AP.

Depending on **AP_1-S3** the CGB board in slot 11 can either belong to CLM_0 or CLM_1. The CGB board in slot 22 always belongs to CLM_1.

Table 9. Address information for GSS and CLM X11.

Acronym	Full name	Connector	Pin	AP_pin
AP_1-S0	Column start position, bit 0	X11	A01	10
AP_1-S1	Column start position, bit 1	X11	B01	9
AP_1-S2	Column start position, bit 2	X11	D01	8
AP_1-S3	0 = CLM-0 1 = CLM-1 (CGB in slot 11)	X11	E01	7
AP_1-SP	Even parity S3-S0	X11	A02	6
AP_3-S0	Row position, bit 0	X11	B02	10
AP_3-S1	Row position, bit 1	X11	D02	9
AP_3-S2	CDM magazine indicator	X11	E02	8
AP_3-S3	bit 3 (Not used)	X11	A03	7
AP_3-SP	Even parity S3-S0	X11	B03	6

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Kontr - Checked		Rev		File
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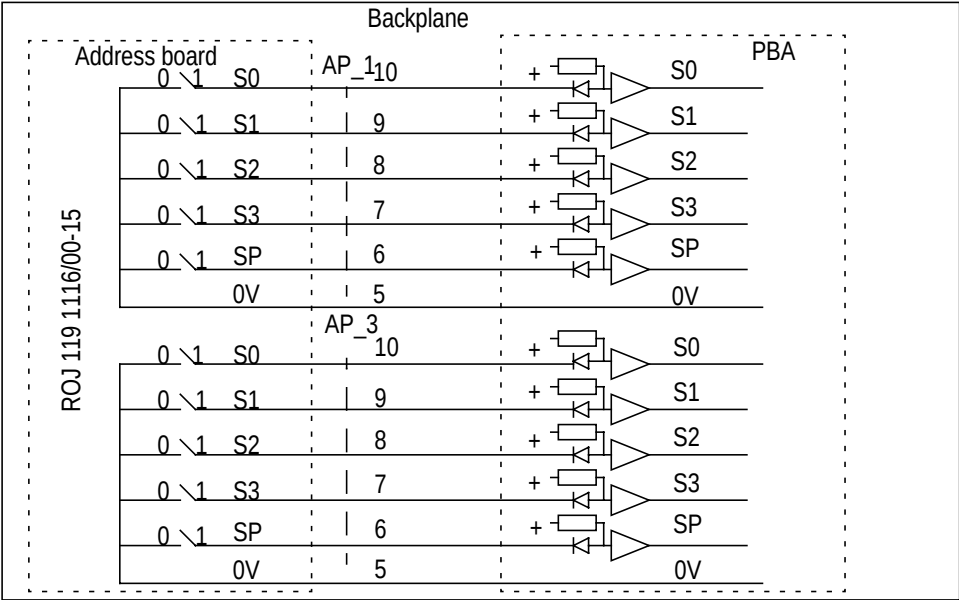


Fig.16. AP_1 and AP_3 implementation

9.2.4 Switch board addresses and plane-id

There are 8 switch boards per plane in a 128K switch.

In a normal case these will be placed in 8 magazines, 16K in each magazine.

Regarding NNRP, the GEM magazine has following possibilities;

- XDB mixed¹ with XNB (max 32K)
XDB with board address **1, 24**
XNB with board address **5, 8 and 16, 19**
 - Pure² NNRP (48K)
XNB with board address **2,5,8 and 13,16,19**
- (1) Mixed versions are not planned for GEM
- (2) Maximum 32K will be introduced, board address **2, 5 and 13, 16**

Switch board address and plane-id are decoded from a combination of the board address (slot position) and the address plug value (AP-1) **by the RP.** (see section Table 68. on page 73)

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.	
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		File	

Table 10. Switch Board Address

Physical pos	Board Address	Board type	Logical switch board
8	1	XDB	AP_1, plane A
11	2	XNB	AP_1, plane A
20	5	XNB	AP_1+1, plane A
29	8	XNB	AP_1+2, plane A
44	13	XNB	AP_1, plane B
53	16	XNB	AP_1+1, plane B
62	19	XNB	AP_1+2, plane B
77	24	XDB	AP_1, plane B

9.2.5

Board address

Board addresses are numbered from 0 to (n-1) for each available slot from left to right.

The board address is taken from the backplane for each board (separated from MB address). An address pin connected to ground in the backplane = "0". An open circuit address pin = "1". Five address pins and one parity pin are used, which allow maximum 32 boards to be addressed see figure 17. Odd parity is used.

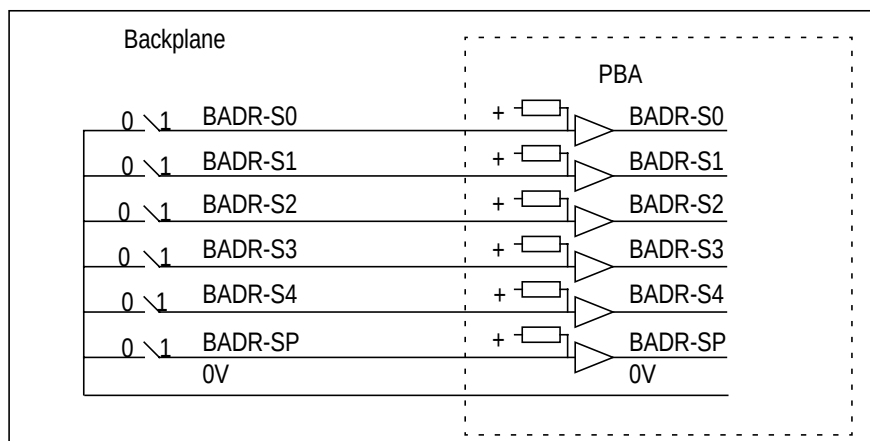
Note !!!! Compared to GDM, GEM will only use a five bit address.

Table 11. Board address information (pin-out) X11

Acronym	Full name	Connector	Pin
BADR-S0	Board address, bit 0	X11	D03
BADR-S1	Board address, bit 1	X11	E03
BADR-S2	Board address, bit 2	X11	A04
BADR-S3	Board address, bit 3	X11	B04
BADR-S4	Board address, bit 4	X11	D04
BADR-SP	Board address, odd parity	X11	E04

see section Table 68. on page 73.

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.		102 62 - BFD 508002/1 Uen	
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**Fig.17. Board address implementation**

9.2.6 Layout information

No special requirements

9.3 TEST AND PROGRAM CONNECTOR BUS

To enable test and program on subsystem level all PBAs in GEM are accessible via AP_2.

Table 12. AP_2 pin out

Acronym	Full name	From Connector	Pin	To Connector	Pin	SCB term pin
3.3V	MBA_3V	AP_2	1	X0201	D05 E05	
FWZ	Flash Write	AP_2	2	X11	E06	
FWPEZ	Flash Write Protect enable	AP_2	3	X11	D07	
MB_WC	MB write Control	AP_2	4	X01	B01	
GND	GND	AP_2	5			
JTAG2_PTMS	Test Mode Select	AP_2	6	X01	E03	B06
JTAG2_PTDI	Test Data Input	AP_2	7	X01	D03	D06
JTAG2_PTDO	Test Data Output	AP_2	8	X01	D04	E06
JTAG2_PTRST	Test Reset	AP_2	9	X01	E01	-
JTAG2_PTCK	Test Clock	AP_2	10	X01	D01	A06

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.			
		102 62 - BFD 508002/1 Uen			
Dokansv/Godkänd - Doc respons/Approved		Kontr - Checked			
		Datum - Date		Rev	
		2001-12-13		D	
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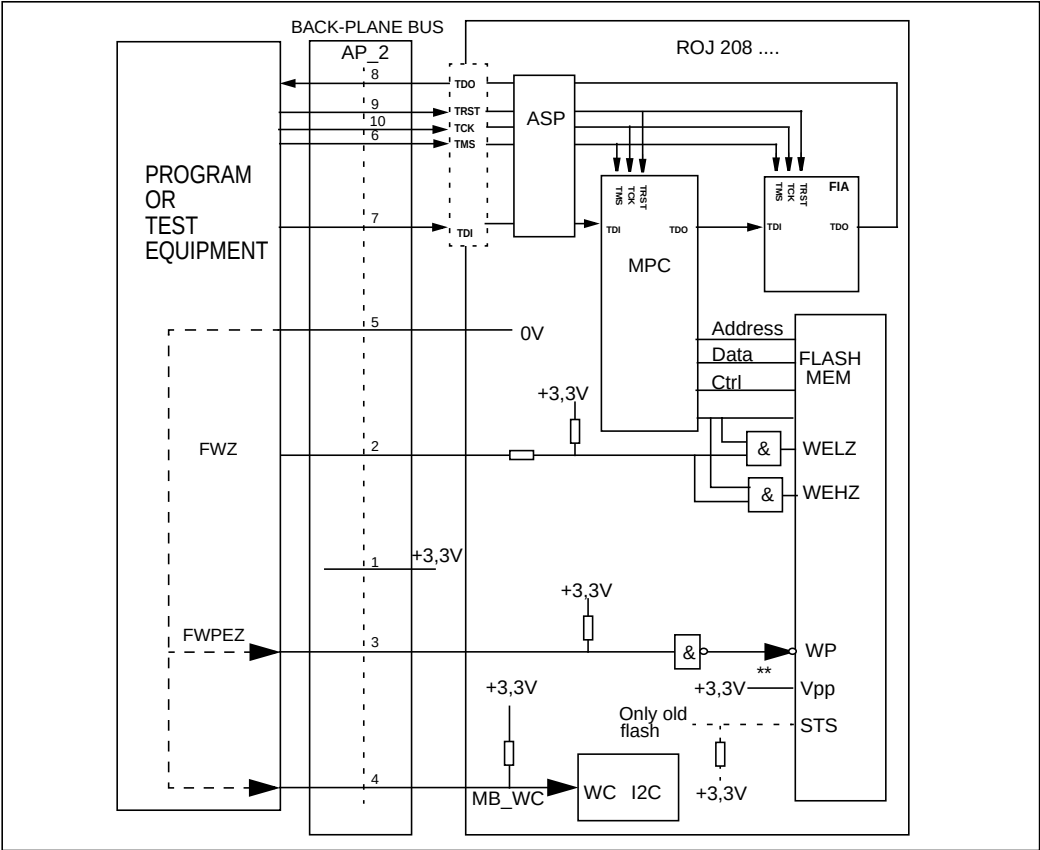


Fig.18. Backplane connection

9.4 MAINTENANCE BUS

The SCB-RP provides the maintenance bus interface. This is implemented as a normal I2C bus. The SCB-RP board acts as the master on this bus, but has also a slave interface like all other boards in the GEM magazine. The maintenance bus also gives the possibility to point out faulty boards in a magazine by controlling a LED (MIA).

The maintenance components on each board are powered and supervised by SCB-RP. The M-bus is not implemented with redundancy. See Table 13 for M-bus address - Slot position.

The address is the same as the board address but the information is separated in the backplane.

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)

Nr - No.

102 62 - BFD 508002/1 Uen

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File

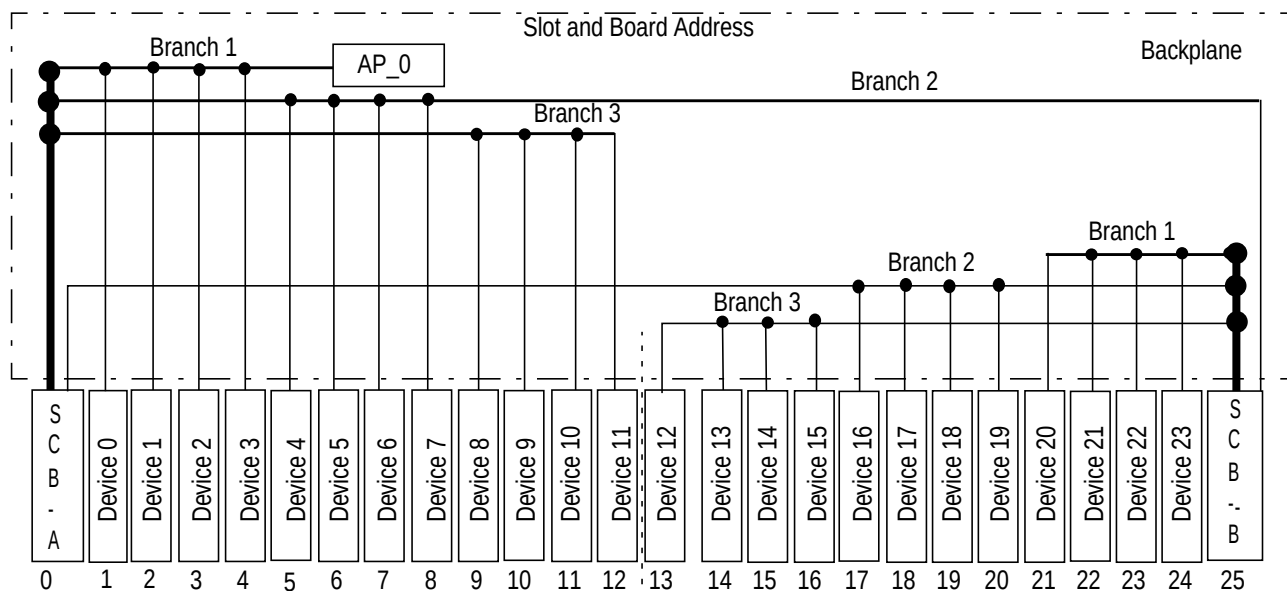


Fig.19. M-bus implementation

Table 13. M-bus address

Slot in GEM M-bus address	AP_0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Physical position	00 55	0 2	0 8	1 1	1 4	1 7	2 0	2 3	2 6	2 9	3 2	3 5	3 8	4 1	4 4	4 7	5 0	5 3	5 6	5 9	6 2	6 5	6 8	7 1	7 4	7 7	8 0
MB_A0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
MB_A1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
MB_A2	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
MB_A3	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1
MB_A4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
SCB - A branch >	1	-	1	1	1	1	2	2	2	2	3	3	3	3	-	-	-	-	-	-	-	-	-	-	-	-	2
SCB - B branch >		2	-	-	-	-	-	-	-	-	-	-	-	-	3	3	3	3	2	2	2	2	1	1	1	1	-

9.4.1

M-bus pin-out

Table 14. SCB-RP Master pin-out X01

Acronym	Full name	Connector	Pin
MB()_SCL<1>	M-bus Serial Clock out 1	X01	A07
MB()_SDA<1>	M-bus Serial Data out 1	X01	D07
MB()_SCL<2>	M-bus Serial Clock out 2	X01	A08
MB()_SDA<2>	M-bus Serial Data out 2	X01	D08
MB()_SCL<3>	M-bus Serial Clock out 3	X01	A09

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Acronym	Full name	Connector	Pin
MB()_SDA<3>	M-bus Serial Data out 3	X01	D09
MB()_3V	3.3 V Power Supply	X01	D05
MB()_3V	3.3 V Power Supply	X01	E05

() = A or B

Table 15. Slave pin-out X01 all boards

Acronym	Full name	Connector	Pin
MB()_SCL<n>	Serial Clock	X01	A04
MB()_SDA<n>	Serial Data	X01	B03
MB()_3V	3.3 V	X01	B04
MB_WC	Write control	X01	B01
MB_A0	Address A0	X01	A02
MB_A1	Address A1	X01	B02
MB_A2	Address A2	X01	D02
MB_A3	Address A3	X01	E02
MB_A4	Address A4	X01	A03

() = A or B

See address in Table 13

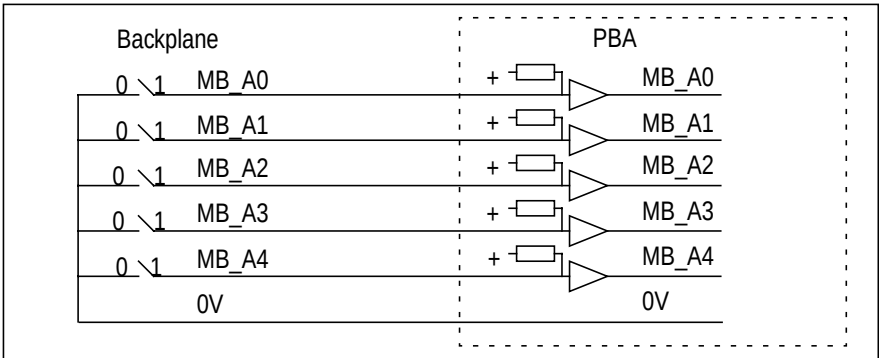


Fig.20. MB address implementation

9.4.2 Maintenance bus control

To enable programming of maintenance data on sub system level, the write control signal AP_2 pin 4 must be connected to GND.

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				File

(MB_WC see figure 18)

SCB-RP_A control dev 0 - 11 and SCB-RP_B and

SCB-RP_B control dev 12 - 23 and SCB-RP_A

9.4.3Layout information

The conductor width for the 3,3V distribution shall be chosen for a short current of 3 A.

9.5SHORT PINS

For each board there will be two backplane connectors, one in the top and one in the bottom that have shorter pins in one row. One top-pin is connected with one bottom-pin see figure 21.

Remaining pins shall **not** be used for normal purpose.

All internal interfaces to/from a board must be inactive until both these pins are connected (top, bottom). This should especially be noted for the RPI parts.

Normal pin = 6,25 mm (earlier figures 5,15 mm and 4,75 mm)

Short pin = 5,15 mm (earlier figures 4,25 mm and 4,75 mm)

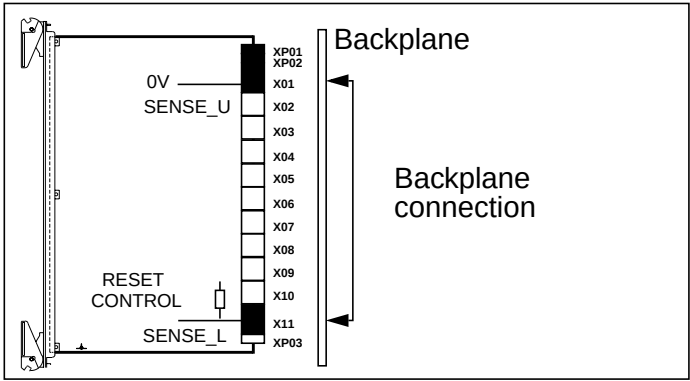


Fig.21. Short pin implementation

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.	102 62 - BFD 508002/1 Uen	
Dokansv/Godkänd - Doc respons/Approved	Kontr - Checked	Datum - Date	Rev	File
		2001-12-13	D	

9.5.1 Short pin pin-out

Table 16. pin-out

Acronym	Full name	Connector	Pin
SENSE_U	SENSE Upper	X01	A01
-		X01	B01
-		X01	D01
-		X01	E01
SENSE_L	SENSE Lower	X11	A10
-		X11	B10
-		X11	D10
-		X11	E10

9.5.1.1 Layout information:

No special requirements

9.6 RPB-S

For communication with the CP, SCB-RP provides a RPB-S interface.

RPB-S is connected to the SCB-RP via a front connector and distributed to the backplane. The front connection is of differential type while the connections towards the backplane are single ended.

Each RPI in the magazine is connected to two RPB-S/M branches, since there exist two SCB-RP boards in a GEM one handling path A (RPB-S/M-A) and the other path B (RPB-S/M-B).

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Dokansv/Godkänd - Doc respons/Approved		Kontr - Checked		Datum - Date	
		2001-12-13		Rev	
		D		File	

The RPB/M distribution is split into 4 branches, each handle up to seven boards.

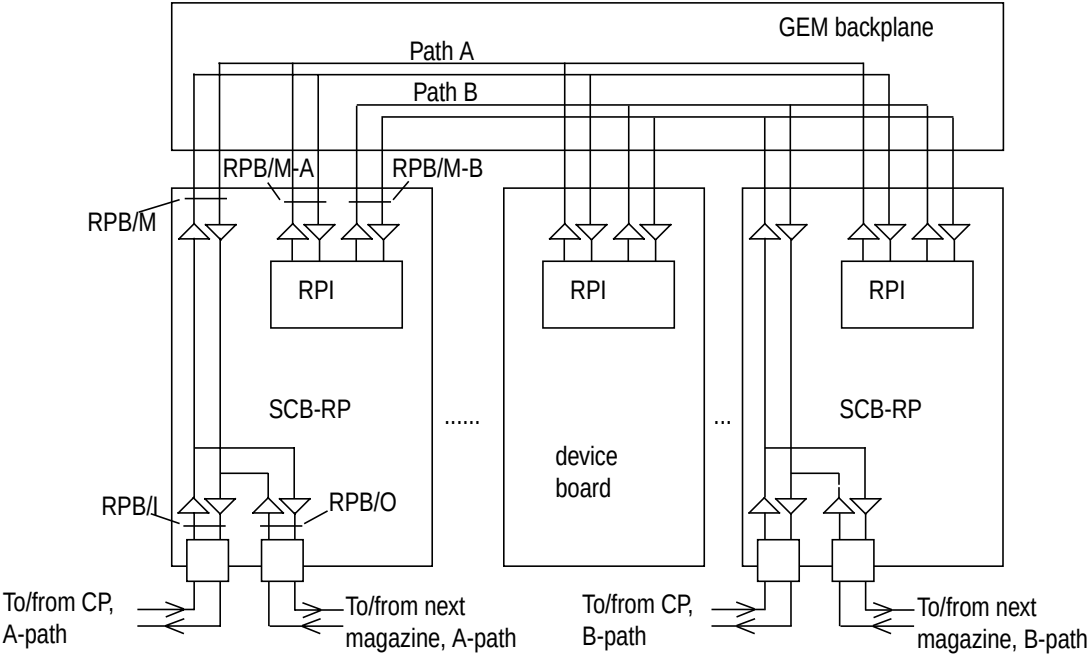


Fig.22. Logical view of one branch

Slot in GEM Branch	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Physical position	02	08	11	14	17	20	23	26	29	32	35	38	41	44	47	50	53	56	59	62	65	68	71	74	77	80
SCB - A branch 1	1	1	1	1	1	1	1																			
SCB - A branch 2								2	2	2	2	2	2	2												
SCB - A branch 3															3	3	3	3	3	3						
SCB - A branch 4																					4	4	4	4	4	4
SCB - B branch 1																					1	1	1	1	1	1
SCB - B branch 2														2	2	2	2	2	2	2						
SCB - B branch 3								3	3	3	3	3	3													
SCB - B branch 4	4	4	4	4	4	4																				
BOARD	S C B - A	X D B - A	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	D E V	X D B - B	S C B - B

Table 17. Branch implementation

Uppgjord (även faktaansvarig om annan) - Prepared (also subject responsible if other)		Nr - No.	102 62 - BFD 508002/1 Uen	
Dokansv/Godkänd - Doc respons/Approved	Kontr - Checked	Datum - Date	Rev	File
		2001-12-13	D	

9.6.1 RPB-S Master Pin-out

Connector X10 contains the RPB-S signals. Note that the name (TX/RX) indicates what the signal is used for from the CP's point of view.

Table 18. RPB-S master pin-out X10 (SCB-RP)

Acronym	Full name	Connector	Pin
RPB/M()_TX<1>	Branch 1 TX	X10	A07
RPB/M()_RX<1>	Branch 1 RX	X10	A08
RPB/M()_TX<2>	Branch 2 TX	X10	B07
RPB/M()_RX<2>	Branch 2 RX	X10	B08
RPB/M()_TX<3>	Branch 3 TX	X10	D07
RPB/M()_RX<3>	Branch 3 RX	X10	D08
RPB/M()_TX<4>	Branch 4 TX	X10	E07
RPB/M()_RX<4>	Branch 4 RX	X10	E08

() = A or B

Table 19. Slave pin-out X10 (all)

Acronym	Full name	Connector	Pin
RPB/M-A_TX<n>	RP A Branch n TX	X10	B09
RPB/M-A_RX<n>	RP A Branch n RX	X10	B10
RPB/M-B_TX<n>	RP B Branch n TX	X10	D09
RPB/M-B_RX<n>	RP B Branch n RX	X10	D10

9.6.1.1 Layout information

Note !!!! The SCB-RP output and the DEV inputs have the same name "TX" and the DEV outputs and SCB-RP input have the same name "RX".

Due to the bus structure, the conductor length for TX/RX shall be matched between the master and slave to avoid reflections in the same branch.

Impedance matching = All signal traces for the RPB-S, shall have a characteristic impedance of 56ohm (>50 ohm). In the backplane, the device shall be connected individually to one central point on a branch and from there to the SCB-RP position.

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Dokansv/Godkänd - Doc respons/Approved	Kontr - Checked	Datum - Date	Rev	File
		2001-12-13	D	

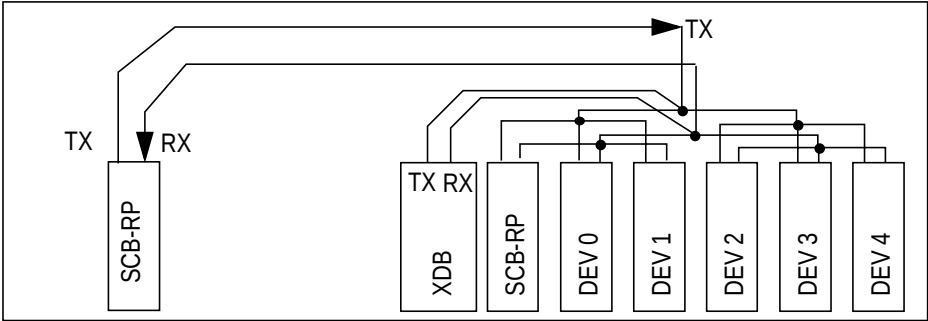


Fig.23. One branch layout example

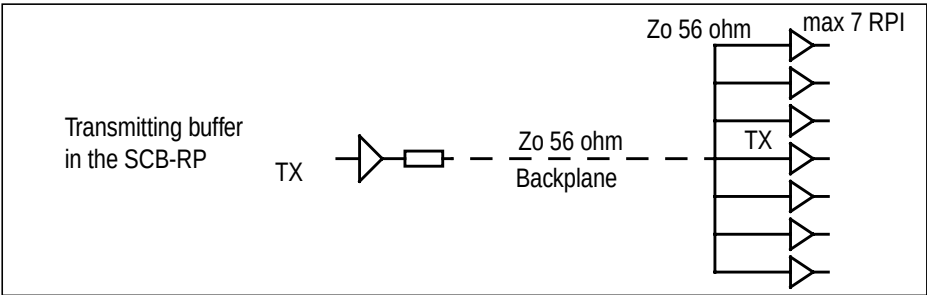


Fig.24. Signals SCB - RP-RPI

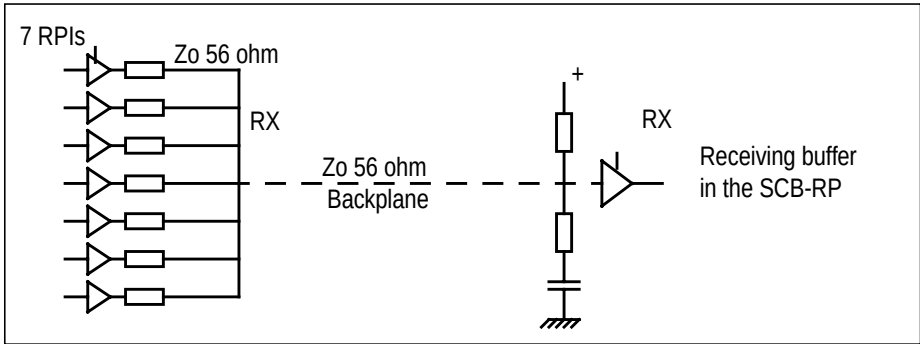


Fig.25. Signals RPI - SCB-RP

9.7 ETHERNET

The SCB-RP provides accessibility to all boards via ethernet. The ethernet is going to be used for verification purposes. It also is prepared for potential future use like RP-RP communication or CP-RP communication.

The SCB-RP board houses an ethernet switch which can provide each board with a 10Mb/s or 100Mb/s ethernet via the backplane.

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		102 62 - BFD 508002/1 Uen			
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		Datum - Date		Rev	
		2001-12-13		D	
				File	

Todays RPI has two 10Mb/s ports, one between each SCB-RP. Compared to GAM, the interface towards the backplane is of standard type 10BASE-T and will use two differential pairs. The pairs are placed to enable device boards to also use the previous interface Ethernet lite.

For next generation SCB-RP, GEM provide additional two pairs for future use of 1GBit/s ethernet. For this project, these signals will only exist in the backplane.

If a DEVICE board shall be used for both ethernet lite and 10BASE-T, following strap field (resistors) must be implemented on the board, see figure below.

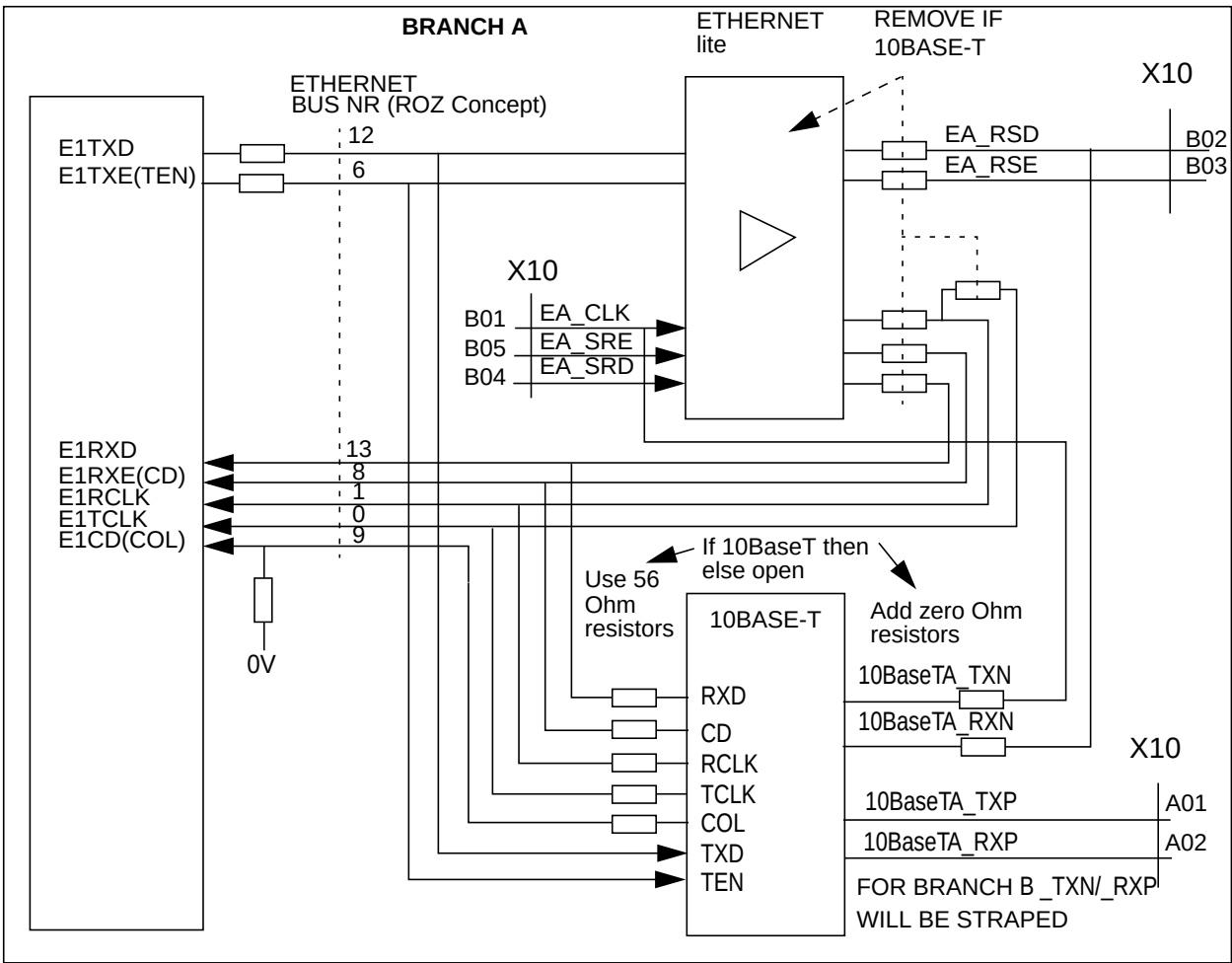


Fig.26. Strap field (resistors) for Ethernet branch A & B

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When change to 10BaseT remove 74LVT16244 and add resistors

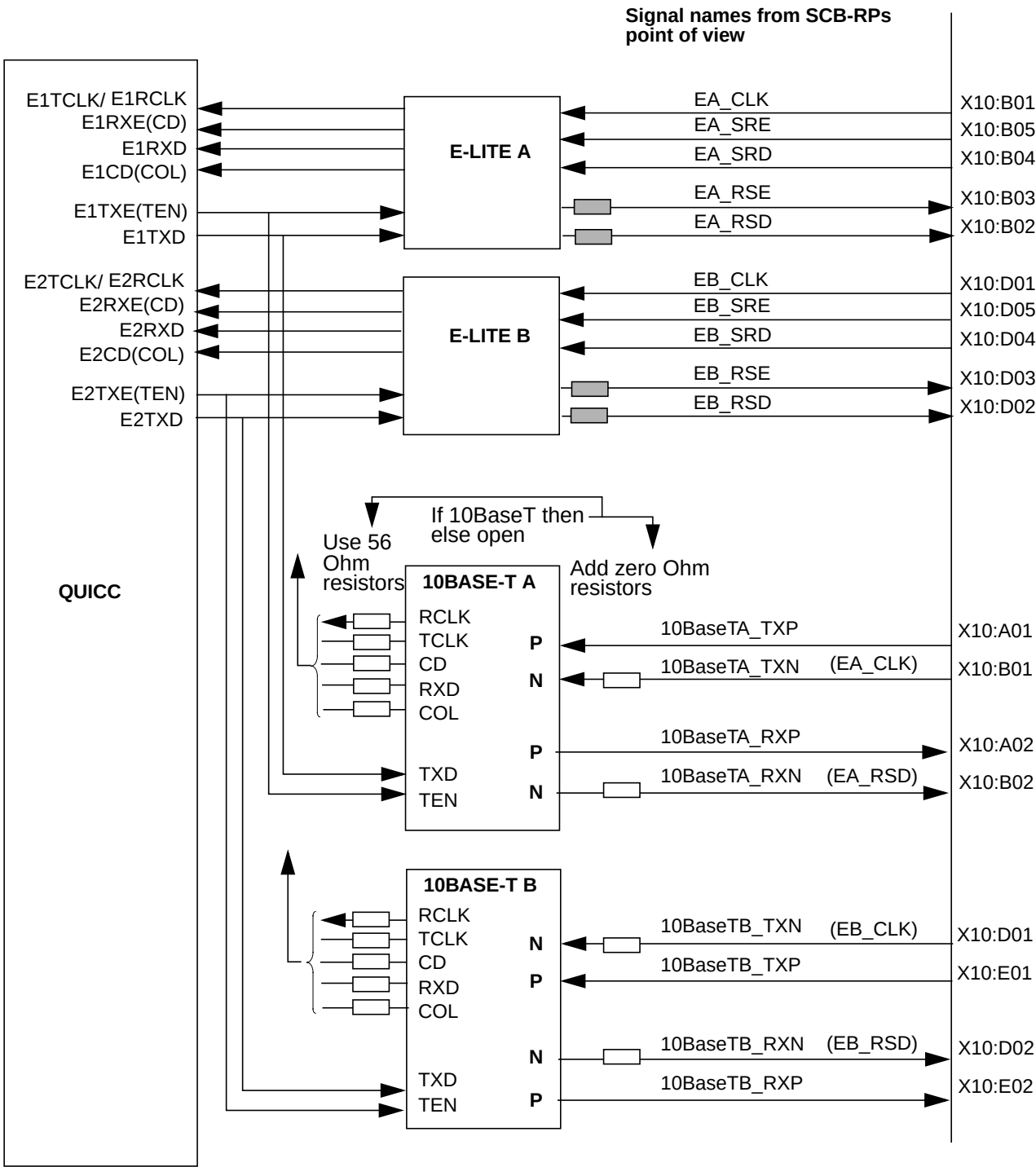
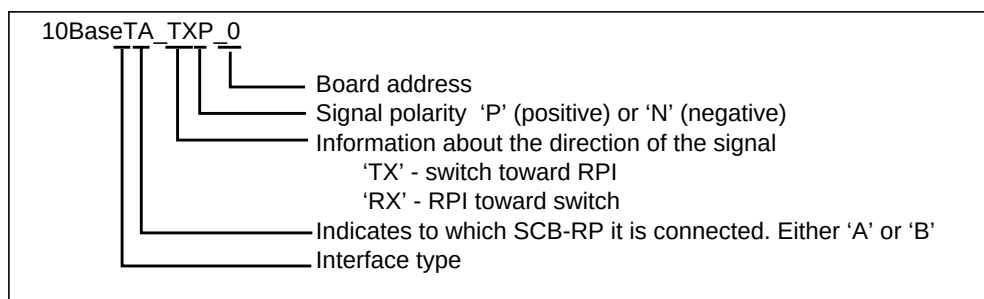


Fig.27. Logical view of the ethernet implementation.

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**Fig.28. Ethernet name description**

9.7.1 Ethernet Master pin-out SCB-RP

Signal names from the SCB-RPs point of view.

Table 20. Master pin out 10Base-T

Acronym		Full name	Connector	Pin_P	Pin_N
10BaseT_TXP_0	10BaseT_TXN_0	Transmit Data ch 0	X06_D	A01	B01
10BaseT_RXP_0	10BaseT_RXN_0	Receive Data ch 0	X06_D	A02	B02
10BaseT_TXP_1	10BaseT_TXN_1	Transmit Data ch 1	X06_D	A03	B03
10BaseT_RXP_1	10BaseT_RXN_1	Receive Data ch 1	X06_D	A04	B04
10BaseT_TXP_2	10BaseT_TXN_2	Transmit Data ch 2	X06_D	A05	B05
10BaseT_RXP_2	10BaseT_RXN_2	Receive Data ch 2	X06_D	A06	B06
10BaseT_TXP_3	10BaseT_TXN_3	Transmit Data ch 3	X06_D	A07	B07
10BaseT_RXP_3	10BaseT_RXN_3	Receive Data ch 3	X06_D	A08	B08
10BaseT_TXP_4	10BaseT_TXN_4	Transmit Data ch 4	X06_D	A09	B09
10BaseT_RXP_4	10BaseT_RXN_4	Receive Data ch 4	X06_D	A10	B10
10BaseT_TXP_5	10BaseT_TXN_5	Transmit Data ch 5	X07_D	A01	B01
10BaseT_RXP_5	10BaseT_RXN_5	Receive Data ch 5	X07_D	A02	B02
10BaseT_TXP_6	10BaseT_TXN_6	Transmit Data ch 6	X07_D	A03	B03
10BaseT_RXP_6	10BaseT_RXN_6	Receive Data ch 6	X07_D	A04	B04
10BaseT_TXP_7	10BaseT_TXN_7	Transmit Data ch 7	X07_D	A05	B05
10BaseT_RXP_7	10BaseT_RXN_7	Receive Data ch 7	X07_D	A06	B06
10BaseT_TXP_8	10BaseT_TXN_8	Transmit Data ch 8	X07_D	A07	B07
10BaseT_RXP_8	10BaseT_RXN_8	Receive Data ch 8	X07_D	A08	B08
10BaseT_TXP_9	10BaseT_TXN_9	Transmit Data ch 9	X07_D	A09	B09
10BaseT_RXP_9	10BaseT_RXN_9	Receive Data ch 9	X07_D	A10	B10

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Acronym		Full name	Connector	Pin_P	Pin_N
10BaseT_TXP_10	10BaseT_TXN_10	Transmit Data ch 10	X08_D	A01	B01
10BaseT_RXP_10	10BaseT_RXN_10	Receive Data ch 10	X08_D	A02	B02
10BaseT_TXP_11	10BaseT_TXN_11	Transmit Data ch 11	X08_D	A03	B03
10BaseT_RXP_11	10BaseT_RXN_11	Receive Data ch 11	X08_D	A04	B04
10BaseT_TXP_12	10BaseT_TXN_12	Transmit Data ch 12	X08_D	A05	B05
10BaseT_RXP_12	10BaseT_RXN_12	Receive Data ch 12	X08_D	A06	B06
10BaseT_TXP_13	10BaseT_TXN_13	Transmit Data ch 13	X08_D	A07	B07
10BaseT_RXP_13	10BaseT_RXN_13	Receive Data ch 13	X08_D	A08	B08
10BaseT_TXP_14	10BaseT_TXN_14	Transmit Data ch 14	X08_D	A09	B09
10BaseT_RXP_14	10BaseT_RXN_14	Receive Data ch 14	X08_D	A10	B10
10BaseT_TXP_15	10BaseT_TXN_15	Transmit Data ch 15	X09_D	A01	B01
10BaseT_RXP_15	10BaseT_RXN_15	Receive Data ch 15	X09_D	A02	B02
10BaseT_TXP_16	10BaseT_TXN_16	Transmit Data ch 16	X09_D	A03	B03
10BaseT_RXP_16	10BaseT_RXN_16	Receive Data ch 16	X09_D	A04	B04
10BaseT_TXP_17	10BaseT_TXN_17	Transmit Data ch 17	X09_D	A05	B05
10BaseT_RXP_17	10BaseT_RXN_17	Receive Data ch 17	X09_D	A06	B06
10BaseT_TXP_18	10BaseT_TXN_18	Transmit Data ch18	X09_D	A07	B07
10BaseT_RXP_18	10BaseT_RXN_18	Receive Data ch 18	X09_D	A08	B08
10BaseT_TXP_19	10BaseT_TXN_19	Transmit Data ch19	X09_D	A09	B09
10BaseT_RXP_19	10BaseT_RXN_19	Receive Data ch 19	X09_D	A10	B10
10BaseT_TXP_20	10BaseT_TXN_20	Transmit Data ch 20	X10_D	A01	B01
10BaseT_RXP_20	10BaseT_RXN_20	Receive Data ch 20	X10_D	A02	B02
10BaseT_TXP_21	10BaseT_TXN_21	Transmit Data ch 21	X10_D	A03	B03
10BaseT_RXP_21	10BaseT_RXN_21	Receive Data ch 21	X10_D	A04	B04
10BaseT_TXP_22	10BaseT_TXN_22	Transmit Data ch 22	X10_D	A05	B05
10BaseT_RXP_22	10BaseT_RXN_22	Receive Data ch 22	X10_D	A06	B06
10BaseT_TXP_23	10BaseT_TXN_23	Transmit Data ch 23	X10_D	A07	B07
10BaseT_RXP_23	10BaseT_RXN_23	Receive Data ch 23	X10_D	A08	B08
10BaseT_TXP_24	10BaseT_TXN_24	Transmit Data ch 24	X10_D	A09	B09
10BaseT_RXP_24	10BaseT_RXN_24	Receive Data ch 24	X10_D	A10	B10
10BaseT_TXP_25	10BaseT_TXN_25	Transmit Data ch 25	X11_D	A01	B01
10BaseT_RXP_25	10BaseT_RXN_25	Receive Data ch 25	X11_D	A02	B02

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Table 21. Master pin out 1000Base-T (for future use)

Acronym		Full name	Connector	Pin_P	Pin_N
1000BaseT_TXP_0	1000BaseT_TXN_0	Transmit Data ch 0	X06_D	D01	E01
1000BaseT_RXP_0	1000BaseT_RXN_0	Receive Data ch 0	X06_D	D02	E02
1000BaseT_TXP_1	1000BaseT_TXN_1	Transmit Data ch 1	X06_D	D03	E03
1000BaseT_RXP_1	1000BaseT_RXN_1	Receive Data ch 1	X06_D	D04	E04
1000BaseT_TXP_2	1000BaseT_TXN_2	Transmit Data ch 2	X06_D	D05	E05
1000BaseT_RXP_2	1000BaseT_RXN_2	Receive Data ch 2	X06_D	D06	E06
1000BaseT_TXP_3	1000BaseT_TXN_3	Transmit Data ch 3	X06_D	D07	E07
1000BaseT_RXP_3	1000BaseT_RXN_3	Receive Data ch 3	X06_D	D08	E08
1000BaseT_TXP_4	1000BaseT_TXN_4	Transmit Data ch 4	X06_D	D09	E09
1000BaseT_RXP_4	1000BaseT_RXN_4	Receive Data ch 4	X06_D	D10	E10
1000BaseT_TXP_5	1000BaseT_TXN_5	Transmit Data ch 5	X07_D	D01	E01
1000BaseT_RXP_5	1000BaseT_RXN_5	Receive Data ch 5	X07_D	D02	E02
1000BaseT_TXP_6	1000BaseT_TXN_6	Transmit Data ch 6	X07_D	D03	E03
1000BaseT_RXP_6	1000BaseT_RXN_6	Receive Data ch 6	X07_D	D04	E04
1000BaseT_TXP_7	1000BaseT_TXN_7	Transmit Data ch 7	X07_D	D05	E05
1000BaseT_RXP_7	1000BaseT_RXN_7	Receive Data ch 7	X07_D	D06	E06
1000BaseT_TXP_8	1000BaseT_TXN_8	Transmit Data ch 8	X07_D	D07	E07
1000BaseT_RXP_8	1000BaseT_RXN_8	Receive Data ch 8	X07_D	D08	E08
1000BaseT_TXP_9	1000BaseT_TXN_9	Transmit Data ch 9	X07_D	D09	E09
1000BaseT_RXP_9	1000BaseT_RXN_9	Receive Data ch 9	X07_D	D10	E10
1000BaseT_TXP_10	1000BaseT_TXN_10	Transmit Data ch 10	X08_D	D01	E01
1000BaseT_RXP_10	1000BaseT_RXN_10	Receive Data ch 10	X08_D	D02	E02
1000BaseT_TXP_11	1000BaseT_TXN_11	Transmit Data ch 11	X08_D	D03	E03
1000BaseT_RXP_11	1000BaseT_RXN_11	Receive Data ch 11	X08_D	D04	E04
1000BaseT_TXP_12	1000BaseT_TXN_12	Transmit Data ch 12	X08_D	D05	E05
1000BaseT_RXP_12	1000BaseT_RXN_12	Receive Data ch 12	X08_D	D06	E06
1000BaseT_TXP_13	1000BaseT_TXN_13	Transmit Data ch 13	X08_D	D07	E07
1000BaseT_RXP_13	1000BaseT_RXN_13	Receive Data ch 13	X08_D	D08	E08
1000BaseT_TXP_14	1000BaseT_TXN_14	Transmit Data ch 14	X08_D	D09	E09
1000BaseT_RXP_14	1000BaseT_RXN_14	Receive Data ch 14	X08_D	D10	E10
1000BaseT_TXP_15	1000BaseT_TXN_15	Transmit Data ch 15	X09_D	D01	E01

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Acronym		Full name	Connector	Pin_P	Pin_N
1000BaseT_RXP_15	1000BaseT_RXN_15	Receive Data ch 15	X09_D	D02	E02
1000BaseT_TXP_16	1000BaseT_TXN_16	Transmit Data ch 16	X09_D	D03	E03
1000BaseT_RXP_16	1000BaseT_RXN_16	Receive Data ch 16	X09_D	D04	E04
1000BaseT_TXP_17	1000BaseT_TXN_17	Transmit Data ch 17	X09_D	D05	E05
1000BaseT_RXP_17	1000BaseT_RXN_17	Receive Data ch 17	X09_D	D06	E06
1000BaseT_TXP_18	1000BaseT_TXN_18	Transmit Data ch18	X09_D	D07	E07
1000BaseT_RXP_18	1000BaseT_RXN_18	Receive Data ch 18	X09_D	D08	E08
1000BaseT_TXP_19	1000BaseT_TXN_19	Transmit Data ch19	X09_D	D09	E09
1000BaseT_RXP_19	1000BaseT_RXN_19	Receive Data ch 19	X09_D	D10	E10
1000BaseT_TXP_20	1000BaseT_TXN_20	Transmit Data ch 20	X10_D	D01	E01
1000BaseT_RXP_20	1000BaseT_RXN_20	Receive Data ch 20	X10_D	D02	E02
1000BaseT_TXP_21	1000BaseT_TXN_21	Transmit Data ch 21	X10_D	D03	E03
1000BaseT_RXP_21	1000BaseT_RXN_21	Receive Data ch 21	X10_D	D04	E04
1000BaseT_TXP_22	1000BaseT_TXN_22	Transmit Data ch 22	X10_D	D05	E05
1000BaseT_RXP_22	1000BaseT_RXN_22	Receive Data ch 22	X10_D	D06	E06
1000BaseT_TXP_23	1000BaseT_TXN_23	Transmit Data ch 23	X10_D	D07	E07
1000BaseT_RXP_23	1000BaseT_RXN_23	Receive Data ch 23	X10_D	D08	E08
1000BaseT_TXP_24	1000BaseT_TXN_24	Transmit Data ch 24	X10_D	D09	E09
1000BaseT_RXP_24	1000BaseT_RXN_24	Receive Data ch 24	X10_D	D10	E10
1000BaseT_TXP_25	1000BaseT_TXN_25	Transmit Data ch 25	X11_D	D01	E01
1000BaseT_RXP_25	1000BaseT_RXN_25	Receive Data ch 25	X11_D	D02	E02

9.7.2 Ethernet slave pin out all boards

Table 22. Slave pin out 10Base-T

Acronym		Full name	Connector	Pin_P	Pin_N
10BaseTA_TXP_()	10BaseTA_TXN_()	Transmit Data A	X10_M	A01	B01
10BaseTA_RXP_()	10BaseTA_RXN_()	Receive Data A	X10_M	A02	B02
10BaseTB_TXP_()	10BaseTB_TXN_()	Transmit Data B	X10_M	E01	D01
10BaseTB_RXP_()	10BaseTB_RXN_()	Receive Data B	X10_M	E02	D02

() = 0 - 25

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Table 23. Slave pin out 1000Base-T

Acronym		Full name	Connector	Pin_P	Pin_N
1000BaseTA_TXP_()	1000BaseTA_TXN_()	Transmit Data A	X10_M	A03	B03
1000BaseTA_RXP_()	1000BaseTA_RXN_()	Receive Data A	X10_M	A04	B04
1000BaseTB_TXP_()	1000BaseTB_TXN_()	Transmit Data B	X10_M	E03	D03
1000BaseTB_RXP_()	1000BaseTB_RXN_()	Receive Data B	X10_M	E04	D04

() = 0 - 25

9.7.2.1 Layout information

Differential pairs 100Ohm ~50MHz. Minimize crosstalk to NEXT.

9.7.3 Ethernet lite support in GEM

To support ethernet lite in GEM one additional connection is implemented between master and slave (E_SRE).

Table 24. Master pin out E_SRE

Acronym	Full name	Connector	Pin
E_SRE_1	SR Enable	X11_D	A03
E_SRE_2	-"	X11_D	B03
E_SRE_3	-"	X11_D	D03
E_SRE_4	-"	X11_D	E03
E_SRE_5	-"	X11_D	A04
E_SRE_6	-"	X11_D	B04
E_SRE_7	-"	X11_D	D04
E_SRE_8	-"	X11_D	E04
E_SRE_9	-"	X11_D	A05
E_SRE_10	-"	X11_D	B05
E_SRE_11	-"	X11_D	D05
E_SRE_12	-"	X11_D	E05
E_SRE_13	-"	X11_D	A06
E_SRE_14	-"	X11_D	B06
E_SRE_15	-"	X11_D	D06
E_SRE_16	-"	X11_D	E06
E_SRE_17	-"	X11_D	A07
E_SRE_18	-"	X11_D	B07
E_SRE_19	-"	X11_D	D07

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		2001-12-13	D
		File	

Acronym	Full name	Connector	Pin
E_SRE_20	-"	X11_D	E07
E_SRE_21	-"	X11_D	A08
E_SRE_22	-"	X11_D	B08
E_SRE_23	-"	X11_D	D08
E_SRE_24	-"	X11_D	E08
E_SRE_25	-"	X11_D	A09
E_SRE_0	-"	X11_D	B09

Table 25. Slave pin-out E_SRE

Acronym	Full name	Connector	Pin
EA_SRE_(n)	SR Enable	X10_M	B05
EB_SRE_(n)	-"	X10_M	D05

n = 0 - 25

9.8 JTAG AND TEST ACCESS

General PBA information.

In order to support programming, debugging and verification, all PBAs shall have a test interface which provides following functions:

- JTAG
- Power reset.
- Support of P-BIST (trigger pin, test mode pin).
- A write enable for Flash programming.
- GND and 3.3V supply.

JTAG complies with IEEE Std 1149.1. It is used for boundary-scan testing during manufacturing and basic test. (If the JTAG chain contain more then 5 circuits an input-buffer is recommend nearby the connector (JTAG1).

9.8.1 JTAG functionality pin-out (ALL positions)

To support Boundary scan (Board test) for all PBAs, the JTAG access shall be divided into two chains:

Chain 1. For the PBA specific circuit(s) with JTAG

- on PBA level accessible by a test fixture (BS)
- on subsystem level accessible by MTC (BS)

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Chain 2. For the RPI block (QUICC, FIA).

- on PBA level accessible by a test fixture (BS and *)
- on subsystem level accessible by the ASP bus (BS and *)

* = Flash programming (P_BOOT)

9.8.1.1 JTAG chain 1 (test fixture access)

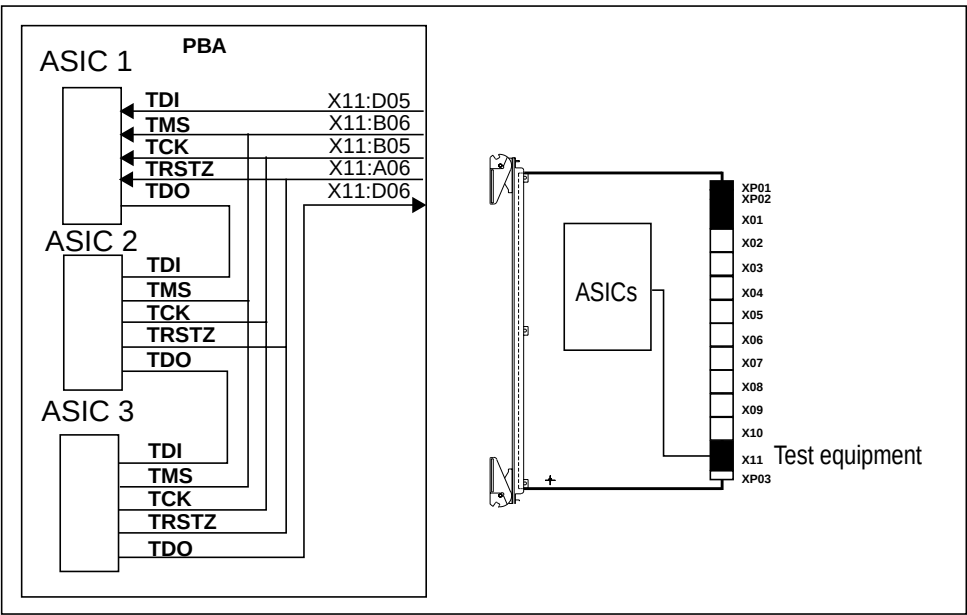


Fig.29. JTAG chain 1

Table 26. JTAG connector 1

Acronym	Full name	Connector	Pin
JTAG1_TCK	Test Clock	X11	B05
JTAG1_TMS	Test Mode Select	X11	B06
JTAG1_TDI	Test Data Input	X11	D05
JTAG1_TDO	Test Data Output	X11	D06
JTAG1_TRSTZ	Test Reset	X11	A06

9.8.1.2 MTC access (subsystem access)

To support the MTC functionality, JTAG chain 1 and the Master Test Controller interface is connected via the backplane

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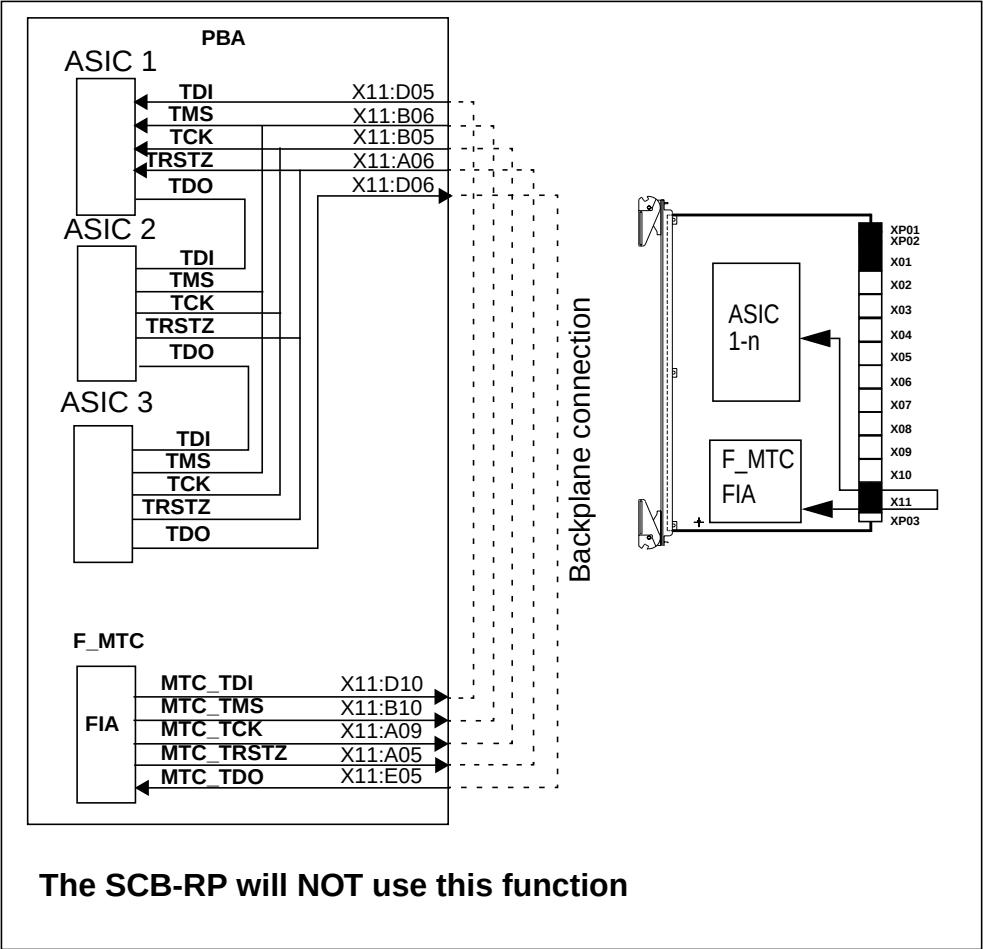


Fig.30. MTC connection

Table 27. MTC pin-out X11 (All positions)

Acronym	Full name	Connector	From Pin	To Pin
MTC_TCK	MTC Test Clock	X11	A09	B05
MTC_TMS	MTC Test Mode Select	X11	B10	B06
MTC_TDI	MTC Test Data Input	X11	D10	D05
MTC_TDO	MTC Test Data Output	X11	E05	D06
MTC_TRSTZ	MTC Test Reset	X11	A05	A06

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		Datum - Date		Rev	
		2001-12-13		D	
				File	

9.8.1.3 JTAG chain 2 (test fixture access)

To support access to the JTAG port on magazine level a multidrop Addressable Scan Port (ASP) transceiver circuit SN74LVT8996 from TI shall be implemented for JTAG chain 2. **It shall be placed nearby X01 and the processor shall be first in chain.**

To guarantee signal quality for the backplane bus, termination will be placed on SCB-RP.

If the PBA is connected to a test fixture **BYPZ** shall be connected to 0V and ASP will be transparent. It is recommended that other programmable circuits shall be placed in this chain (PLD).

In the magazine the PBA will be connected to a test or programming equipment via AP_2 and a bus in the backplane.

The board address is used for access.

In GEM this function will be implemented according to figure 32.

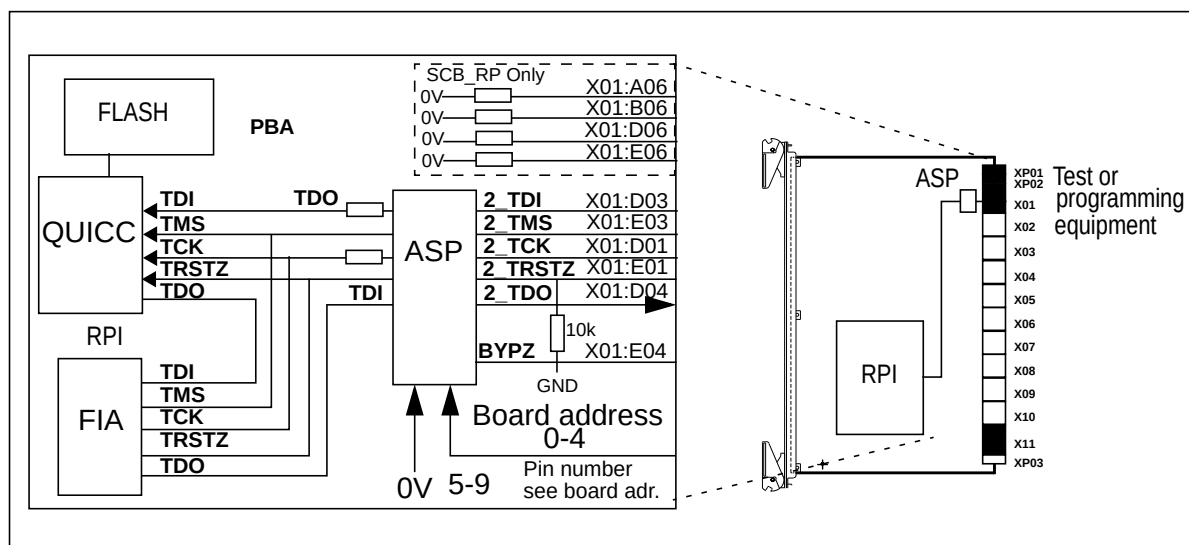


Fig.31. JTAG chain 2

Table 28. JTAG connector 2

Acronym	Full name	Connector	Pin	AP_2 pin	SCB term pin
JTAG2_TMS	Test Mode Select	X01	E03	6	B06
JTAG2_TDI	Test Data Input	X01	D03	7	D06
JTAG2_TDO	Test Data Output	X01	D04	8	E06
JTAG2_TRSTZ	Test Reset	X01	E01	9	-
JTAG2_TCK	Test Clock	X01	D01	10	A06
BYPZ	Bypass ASP	X01	E04		

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				File	

9.8.1.4 TAG chain 2 (subsystem access)

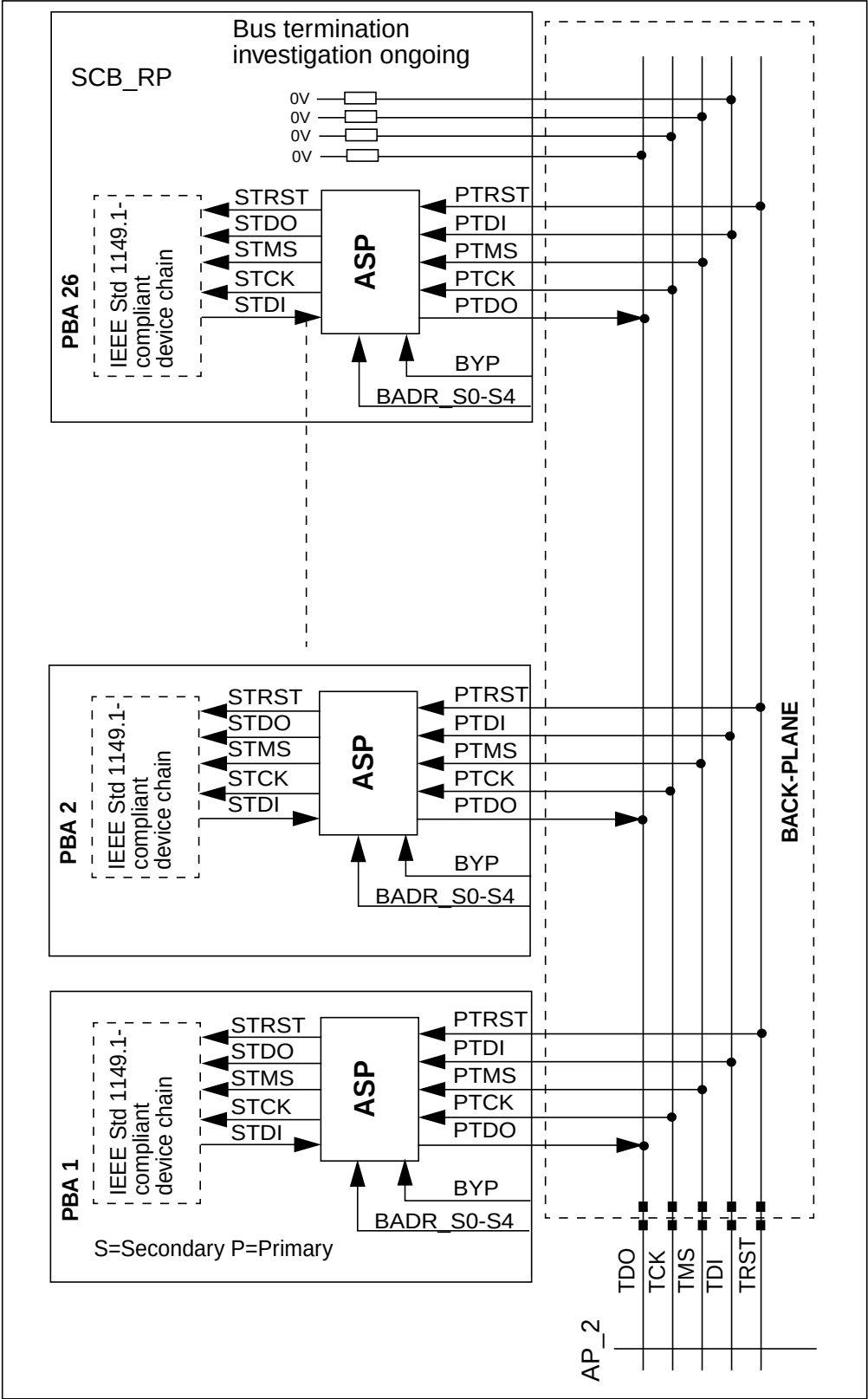


Fig.32. Backplane connection

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		File	

9.8.2 Test Access Port pin-out (All positions)

General PBA information.

The Test Access Port is the interface towards PBA production test (P-BIST). P3V and PGND can be used for external drivers (V24). On the PBA, 10 Ohm shall be put in series with 3,3V.

If Vcc_mon is used, a resistor shall be put in series.

Table 29. TAP-pin out

Acronym	Full name	Connector	Pin
TAP_HRSTZ	Ext. Hard Reset	X11	A07
TRG	Trigger	X11	B07
TMPZ0	Test Mode Pin 0	X11	D08
TMPZ1	Test Mode Pin 1	X11	E08
NC	Not connected	X11	E09
NC	Not connected	X11	E07
FWPEZ	Flash Write Protect enable	X11	D07
P3V	+3.3V	X11	A08
PGND	GND	X11	B08
V24_TX	V24 Transmit Data	X11	B09
V24_RX	V24 Receive Data	X11	D09
FWZ	Flash Write	X11	E06
Vcc_mon	Extra voltage mon.	X11	E10

9.8.2.1 Layout information

No special requirements.

9.8.3 Hardware requirements P-BIST

The P-BIST method requires some special interface to be added on each PBA product. The board shall have a RS 232 interface used for communication between the micro processor on the PBA and TAP (V24_TX, V24_RX). To be able to fault trace with an oscilloscope or logic analyser a trigger reference (TRG) shall be available.

Test Mode Pin (TMP) shall be read at the very beginning of the boot program and in some cases at the beginning of exception handling routines to know if the board is in a test environment (TMP0Z). TMP1Z are aimed for additional selection (free of use).

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A HW reset shall be available for reset of the microprocessor TAP_HRSTZ. This input shall be connected to the reset circuit (voltage monitor).

In connector X10 NC pins can be used as test fixture measuring pins, for example test of on board oscillators see XDB use in Table 66.

9.8.4 Flash programming

The on board boundary scan chain JTAG2 give the possibility, via the QUICC to access the flash memory see pins Table 28. With help of FWZ fast write programming could be used.

FWPEZ enable access to locked blocks (example boot area).

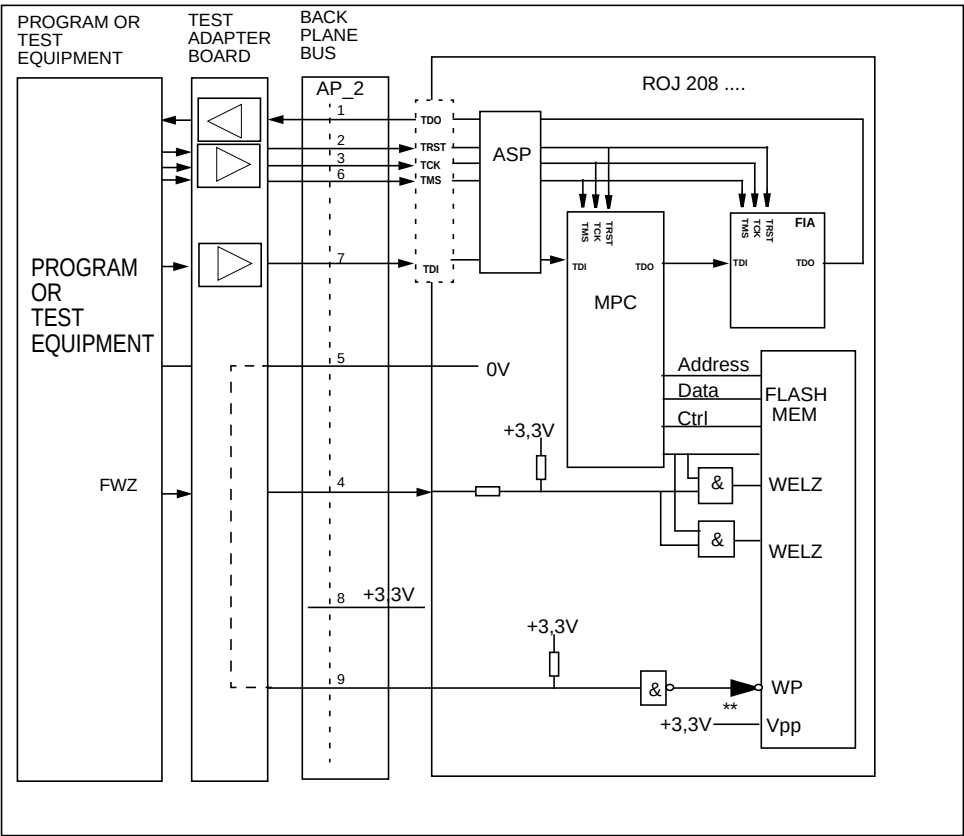


Fig.33. Flash programming via the boundary-scan chain

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				File	

9.9 DL34

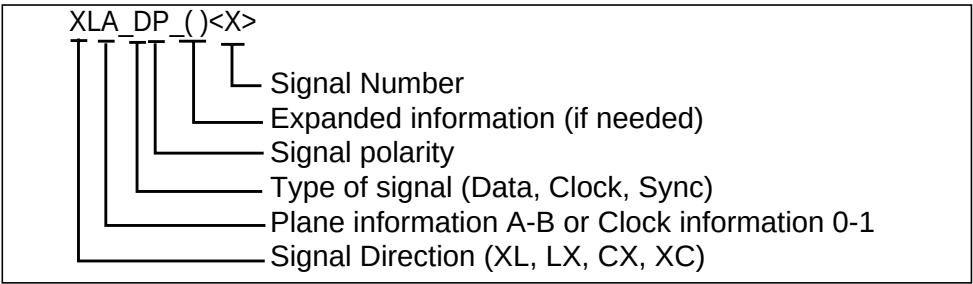


Fig.34. Signal name built-up (switch)

DL34 is the interface between XDBs and DEvIce units (ET155-1, DLEB, CSPB).

The backplane interface is strictly an internal switch interface even if the device boards are connected to it.

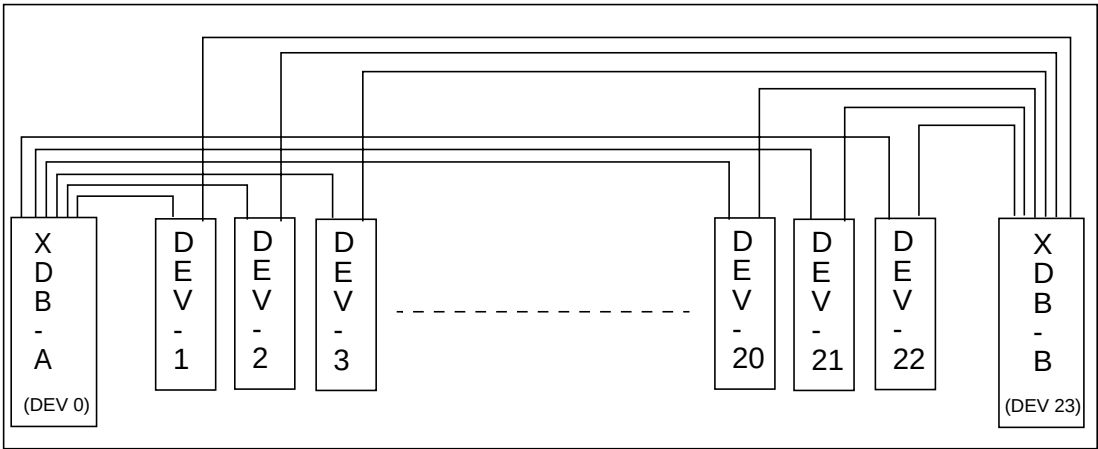


Fig.35. DL34 connection DEV 1 - 22

9.9.1 DL34 XDB Master pin-out

Table 30. DL34 XDB

Acronym		Full name	Connector	Pin	Pin
XL()_DP<0+n>	XL()_DN<0+n>	XL_Data-0+n	X3, X4, X5, X6	A01	B01
XL()_CP<0+n>	XL()_CN<0+n>	XL_Clock-0+n	X3, X4, X5, X6	A02	B02
LX()_DP<0+n>	LX()_DN<0+n>	LX_Data-0+n	X3, X4, X5, X6	A03	B03
XL()_DP<1+n>	XL()_DN<1+n>	XL_Data-1+n	X3, X4, X5, X6	D01	E01
XL()_CP<1+n>	XL()_CN<1+n>	XL_Clock-1+n	X3, X4, X5, X6	D02	E02
LX()_DP<1+n>	LX()_DN<1+n>	LX_Data-1+n	X3, X4, X5, X6	D03	E03

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Acronym		Full name	Connector	Pin	Pin
XL()_DP<2+n>	XL()_DN<2+n>	XL_Data-2+n	X3, X4, X5, X6	A04	B04
XL()_CP<2+n>	XL()_CN<2+n>	XL_Clock-2+n	X3, X4, X5, X6	A05	B05
LX()_DP<2+n>	LX()_DN<2+n>	LX_Data-2+n	X3, X4, X5, X6	A06	B06
XL()_DP<3+n>	XL()_DN<3+n>	XL_Data-3+n	X3, X4, X5, X6	D04	E04
XL()_CP<3+n>	XL()_CN<3+n>	XL_Clock-3+n	X3, X4, X5, X6	D05	E05
LX()_DP<3+n>	LX()_DN<3+n>	LX_Data-3+n	X3, X4, X5, X6	D06	E06
XL()_DP<4+n>	XL()_DN<4+n>	XL_Data-4+n	X3, X4, X5, X6	A07	B07
XL()_CP<4+n>	XL()_CN<4+n>	XL_Clock-4+n	X3, X4, X5, X6	A08	B08
LX()_DP<4+n>	LX()_DN<4+n>	LX_Data-4+n	X3, X4, X5, X6	A09	B09
XL()_DP<5+n>	XL()_DN<5+n>	XL_Data-5+n	X3, X4, X5, X6	D07	E07
XL()_CP<5+n>	XL()_CN<5+n>	XL_Clock-5+n	X3, X4, X5, X6	D08	E08
LX()_DP<5+n>	LX()_DN<5+n>	LX_Data-5+n	X3, X4, X5, X6	D09	E09

() = A or B For **X03** n=n+0 **X04** n=n+6 **X05** n=n+12 **X06** n=n+18(21)

9.9.2 DL34 Slave pin-out X04

Table 31. DL34 <n> = 0-21

Acronym		Full name	Connector	Pin_P	Pin_N
XLA_DP<n>	XLA_DN<n>	XL-Data A	X04	A08	B08
XLA_CP<n>	XLA_CN<n>	XL-Clock A	X04	A09	B09
LXA_DP<n>	LXA_DN<n>	LX-Data A	X04	A10	B10
XLB_DP<n>	XLB_DN<n>	XL-Data B	X04	A01	B01
XLB_CP<n>	XLB_CN<n>	XL-Clock B	X04	A02	B02
LXB_DP<n>	LXB_DN<n>	LX-Data B	X04	A03	B03

9.9.2.1 Layout information

LVDS differential pair 100 Ohm, 222 Mb/s point to point. The signals shall if possible be routed without any via. The differential pairs XL_D,XL_C and LX_D shall be routed in the same way but in different signal layers.

9.10 PROTECTION SWITCH INTERFACE (ET155-1)

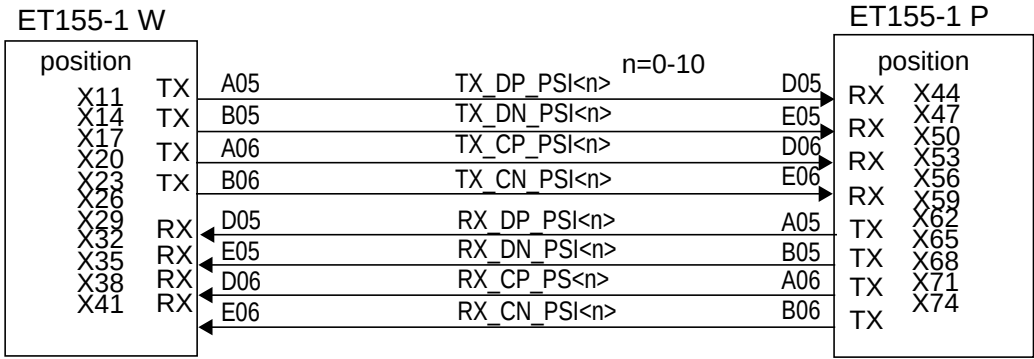
The interface is intended for connection between each pair of Working and Protecting ET-155-1 boards see figure 3. Signal names indicates from the working boards point of view.

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9.10.1 PSI pin out X04

Table 32. ET155-1 PSI (Pin I/O)

Acronym		Full name	Connector	Pin	Pin
TX_DP_PSI<>	TX_DN_PSI<>	Tx Serial Data out	X04	A05	B05
TX_CP_PSI<>	TX_CN_PSI<>	Tx Serial Clock out	X04	A06	B06
RX_DP_PSI<>	RX_DN_PSI<>	Rx Serial Data in	X04	D05	E05
RX_CP_PSI<>	RX_CN_PSI<>	Rx Serial Clock in	X04	D06	E06

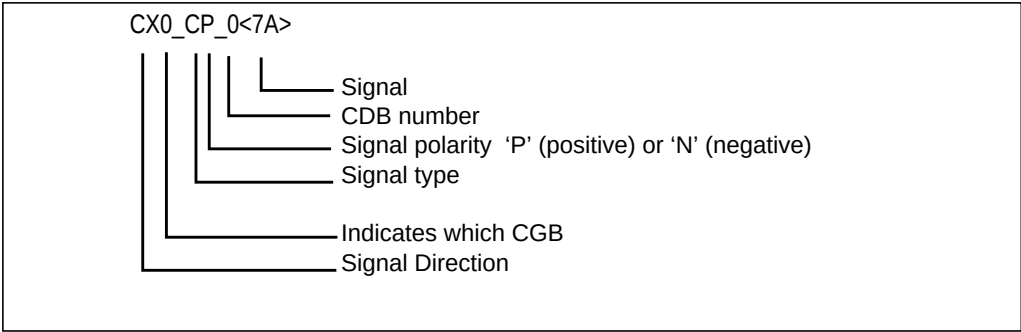


9.10.1.1 Layout information

LVDS differential pair 100 Ohm.

9.11 CLOCK-SIGNALS

Two CGBs (Clock Generation Board) are devoted to perform clock generation and distribution Function. When switch capacity requires more than one GEM, the distribution function is accomplished through CDBs. Network Synchronization Function is spread over one or two IRBs.



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9.11.1 Internal clock distribution CGB, XDB/XNB (16K GEM)

In this case clocks are distributed via the backplane, one XDB and one XNB per plane can be used.

For XNB the clock will be distributed to board address **5** and **16**.

To compensate for Clock distribution in CX direction via cable, the trace length for differential pairs, named CX_C shall be **1,5m**, see bold signals(8) in Table 33.

Fig.36. Internal clock distribution (16K GEM)

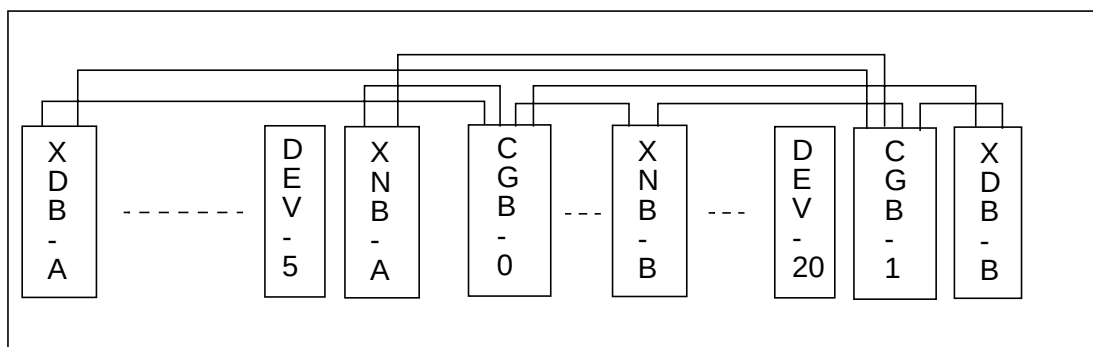


Table 33. CGB_0 and CGB_1 OUTPUT pin-out X2

Acronym		Full name	Connector	Pin_P	Pin_N
CX()_CP<0>	CX()_CN<0>	CLM to X clock	X02	A01	B01
CX()_SP<0>	CX()_SN<0>	CLM to X sync	X02	A02	B02
XC()_SP<0>	XC()_SN<0>	X to CLM sync	X02	A03	B03
CX()_CP<1>	CX()_CN<1>	CLM to X clock	X02	D01	E01
CX()_SP<1>	CX()_SN<1>	CLM to X sync	X02	D02	E02
XC()_SP<1>	XC()_SN<1>	X to CLM sync	X02	D03	E03
CX()_CP<2>	CX()_CN<2>	CLM to X clock	X02	A04	B04
CX()_SP<2>	CX()_SN<2>	CLM to X sync	X02	A05	B05
XC()_SP<2>	XC()_SN<2>	X to CLM sync	X02	A06	B06
CX()_CP<3>	CX()_CN<3>	CLM to X clock	X02	D04	E04
CX()_SP<3>	CX()_SN<3>	CLM to X sync	X02	D05	E05
XC()_SP<3>	XC()_SN<3>	X sync to CLM	X02	D06	E06

() = CGB 0 or 1

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Table 34. XDB A and B INPUT pin-out X01

Acronym		Full name	Connector	Pin_P	Pin_N
CX()_CP<0>	CX()_CN<0>	CLM to X clock	X01	D05	E05
CX()_SP<0>	CX()_SN<0>	CLM to X sync	X01	D06	E06
XC()_SP<0>	XC()_SN<0>	X to CLM sync	X01	D07	E07
CX()_CP<1>	CX()_CN<1>	CLM to X clock	X01	D08	E08
CX()_SP<1>	CX()_SN<1>	CLM to X sync	X01	D09	E09
XC()_SP<1>	XC()_SN<1>	X to CLM sync	X01	D10	E10

() 0 or 1

Table 35. XNB A and B INPUT pin-out X01

Acronym		Full name	Connector	Pin_P	Pin_N
CX()_CP<2>	CX()_CN<2>	CLM to X clock	X01	D05	E05
CX()_SP<2>	CX()_SN<2>	CLM to X sync	X01	D06	E06
XC()_SP<2>	XC()_SN<2>	X to CLM sync	X01	D07	E07
CX()_CP<3>	CX()_CN<3>	CLM to X clock	X01	D08	E08
CX()_SP<3>	CX()_SN<3>	CLM to X sync	X01	D09	E09
XC()_SP<3>	XC()_SN<3>	X to CLM sync	X01	D10	E10

() 0 or 1

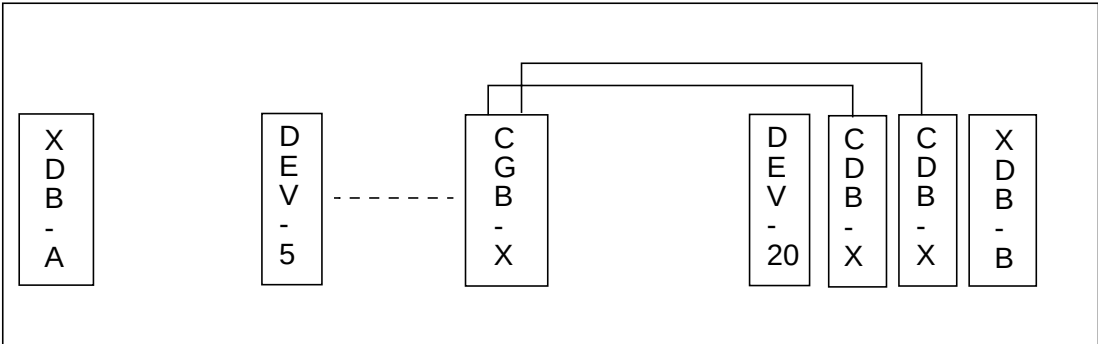
9.11.1.1 Layout information

LVDS differential pair 100 Ohm. (bold signals 1,5 m)

9.11.2 External clock distribution (>16K GEM)

Clocks will be distributed from CDBs in physical position X71 and X74.

Fig.37. External clock distribution



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		Datum - Date		Rev	
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				File	

Table 36. CLOCK/SYNC DISTR. CGB OUTPUT (to CDB_0)

Acronym		Full name	Connector	Pin_P	Pin_N
CX()_CP_0<7>	CX()_CN_0<7>	CLM to CDB clock	M_X02	A07	B07
CX()_SP_0<7>	CX()_SN_0<7>	CLM to CDB sync	M_X02	A08	B08
XC()_SP_0<7>	XC()_SN_0<7>	CDB to CLM sync	M_X02	A09	B09
CX()_CP_0<6>	CX()_CN_0<6>	CLM to CDB clock	M_X02	D07	E07
CX()_SP_0<6>	CX()_SN_0<6>	CLM to CDB sync	M_X02	D08	E08
XC()_SP_0<6>	XC()_SN_0<6>	CDB to CLM sync	M_X02	D09	E09
CX()_CP_0<5>	CX()_CN_0<5>	CLM to CDB clock	M_X02	A10	B10
CX()_SP_0<5>	CX()_SN_0<5>	CLM to CDB sync	M_X06	A01	B01
XC()_SP_0<5>	XC()_SN_0<5>	CDB to CLM sync	M_X06	A02	B02
CX()_CP_0<4>	CX()_CN_0<4>	CLM to CDB clock	M_X02	D10	E10
CX()_SP_0<4>	CX()_SN_0<4>	CLM to CDB sync	M_X06	D01	E01
XC()_SP_0<4>	XC()_SN_0<4>	CDB to CLM sync	M_X06	D02	E02
CX()_CP_0<3>	CX()_CN_0<3>	CLM to CDB clock	M_X06	A03	B03
CX()_SP_0<3>	CX()_SN_0<3>	CLM to CDB sync	M_X06	A04	B04
XC()_SP_0<3>	XC()_SN_0<3>	CDB to CLM sync	M_X06	A05	B05
CX()_CP_0<2>	CX()_CN_0<2>	CLM to CDB clock	M_X06	D03	E03
CX()_SP_0<2>	CX()_SN_0<2>	CLM to CDB sync	M_X06	D04	E04
XC()_SP_0<2>	XC()_SN_0<2>	CDB to CLM sync	M_X06	D05	E05
CX()_CP_0<1>	CX()_CN_0<1>	CLM to CDB clock	M_X06	A06	B06
CX()_SP_0<1>	CX()_SN_0<1>	CLM to CDB sync	M_X06	A07	B07
XC()_SP_0<1>	XC()_SN_0<1>	CDB to CLM sync	M_X06	A08	B08
CX()_CP_0<0>	CX()_CN_0<0>	CLM to CDB clock	M_X06	D06	E06
CX()_SP_0<0>	CX()_SN_0<0>	CLM to CDB sync	M_X06	D07	E07
XC()_SP_0<0>	XC()_SN_0<0>	CDB to CLM sync	M_X06	D08	E08

() = 0 or 1

M_ = Mother connector

D_ = Daughter connector

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Table 37. CLOCK/SYNC DISTR. CGB OUTPUT (to CDB_1)

Acronym		Full name	Connector	Pin_P	Pin_N
CX()_CP_1<7>	CX()_CN_1<7>	CLM to CDB clock	M_X06	A09	B09
CX()_SP_1<7>	CX()_SN_1<7>	CLM to CDB sync	M_X06	A10	B10
XC()_SP_1<7>	XC()_SN_1<7>	CDB to CLM sync	D_X06	A01	B01
CX()_CP_1<6>	CX()_CN_1<6>	CLM to CDB clock	M_X06	D09	E09
CX()_SP_1<6>	CX()_SN_1<6>	CLM to CDB sync	M_X06	D10	E10
XC()_SP_1<6>	XC()_SN_1<6>	CDB to CLM sync	D_X06	D01	E01
CX()_CP_1<5>	CX()_CN_1<5>	CLM to CDB clock	D_X06	A02	B02
CX()_SP_1<5>	CX()_SN_1<5>	CLM to CDB sync	D_X06	A03	B03
XC()_SP_1<5>	XC()_SN_1<5>	CDB to CLM sync	D_X06	A04	B04
CX()_CP_1<4>	CX()_CN_1<4>	CLM to CDB clock	D_X06	D02	E02
CX()_SP_1<4>	CX()_SN_1<4>	CLM to CDB sync	D_X06	D03	E03
XC()_SP_1<4>	XC()_SN_1<4>	CDB to CLM sync	D_X06	D04	E04
CX()_CP_1<3>	CX()_CN_1<3>	CLM to CDB clock	D_X06	A05	B05
CX()_SP_1<3>	CX()_SN_1<3>	CLM to CDB sync	D_X06	A06	B06
XC()_SP_1<3>	XC()_SN_1<3>	CDB to CLM sync	D_X06	A07	B07
CX()_CP_1<2>	CX()_CN_1<2>	CLM to CDB clock	D_X06	D05	E05
CX()_SP_1<2>	CX()_SN_1<2>	CLM to CDB sync	D_X06	D06	E06
XC()_SP_1<2>	XC()_SN_1<2>	CDB to CLM sync	D_X06	D07	E07
CX()_CP_1<1>	CX()_CN_1<1>	CLM to CDB clock	D_X06	A08	B08
CX()_SP_1<1>	CX()_SN_1<1>	CLM to CDB sync	D_X06	A09	B09
XC()_SP_1<1>	XC()_SN_1<1>	CDB to CLM sync	D_X06	A10	B10
CX()_CP_1<0>	CX()_CN_1<0>	CLM to CDB clock	D_X06	D08	E08
CX()_SP_1<0>	CX()_SN_1<0>	CLM to CDB sync	D_X06	D09	E09
XC()_SP_1<0>	XC()_SN_1<0>	CDB to CLM sync	D_X06	D10	E10

() = CGB 0 or 1

M_ = Mother connector

D_ = Daughter connector

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Table 38. CLOCK/SYNC DISTR. CDB INPUT (from CGB)

Acronym		Full name	Connector	Pin_P	Pin_N
CX()_CP_(n)<7>	CX()_CN_(n)<7>	CLM to CDB clock	X04	D01	E01
CX()_SP_(n)<7>	CX()_SN_(n)<7>	CLM to CDB sync	X04	D02	E02
XC()_SP_(n)<7>	XC()_SN_(n)<7>	CDB to CLM sync	X04	D03	E03
CX()_CP_(n)<6>	CX()_CN_(n)<6>	CLM to CDB clock	X04	D08	E08
CX()_SP_(n)<6>	CX()_SN_(n)<6>	CLM to CDB sync	X04	D09	E09
XC()_SP_(n)<6>	XC()_SN_(n)<6>	CDB to CLM sync	X04	D10	E10
CX()_CP_(n)<5>	CX()_CN_(n)<5>	CLM to CDB clock	X07	A01	B01
CX()_SP_(n)<5>	CX()_SN_(n)<5>	CLM to CDB sync	X07	A02	B02
XC()_SP_(n)<5>	XC()_SN_(n)<5>	CDB to CLM sync	X07	A03	B03
CX()_CP_(n)<4>	CX()_CN_(n)<4>	CLM to CDB clock	X07	D01	E01
CX()_SP_(n)<4>	CX()_SN_(n)<4>	CLM to CDB sync	X07	D02	E02
XC()_SP_(n)<4>	XC()_SN_(n)<4>	CDB to CLM sync	X07	D03	E03
CX()_CP_(n)<3>	CX()_CN_(n)<3>	CLM to CDB clock	X07	A04	B04
CX()_SP_(n)<3>	CX()_SN_(n)<3>	CLM to CDB sync	X07	A05	B05
XC()_SP_(n)<3>	XC()_SN_(n)<3>	CDB to CLM sync	X07	A06	B06
CX()_CP_(n)<2>	CX()_CN_(n)<2>	CLM to CDB clock	X07	D04	E04
CX()_SP_(n)<2>	CX()_SN_(n)<2>	CLM to CDB sync	X07	D05	E05
XC()_SP_(n)<2>	XC()_SN_(n)<2>	CDB to CLM sync	X07	D06	E06
CX()_CP_(n)<1>	CX()_CN_(n)<1>	CLM to CDB clock	X07	A07	B07
CX()_SP_(n)<1>	CX()_SN_(n)<1>	CLM to CDB sync	X07	A08	B08
XC()_SP_(n)<1>	XC()_SN_(n)<1>	CDB to CLM sync	X07	A09	B09
CX()_CP_(n)<0>	CX()_CN_(n)<0>	CLM to CDB clock	X07	D07	E07
CX()_SP_(n)<0>	CX()_SN_(n)<0>	CLM to CDB sync	X07	D08	E08
XC()_SP_(n)<0>	XC()_SN_(n)<0>	CDB to CLM sync	X07	D09	E09
GND	GND		X07	A10	B10
GND	GND		X07	D10	E10

() = 0 or 1 (CGB) (n) = 0 or 1 (CDB)

9.11.2.1 Layout information

LVDS differential pair 100 Ohm.

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		File	

9.11.3 Incoming reference signals

From each IRB three PAIRS OF LVDS sync signals are distributed to CGB_0 and CGB_1.

Fig.38. Sync distribution

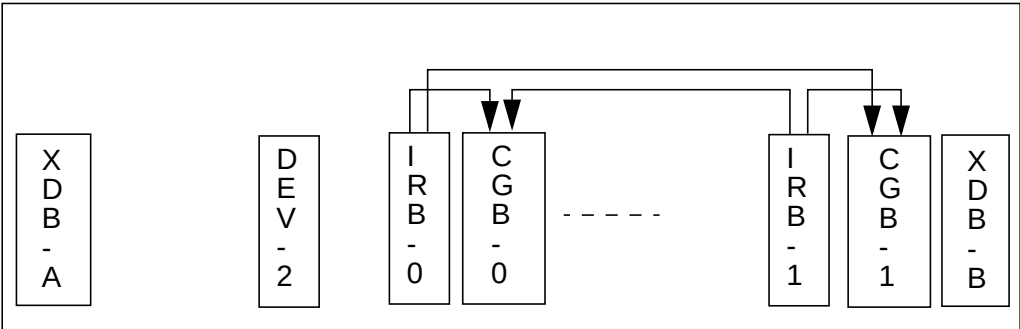


Table 39. IRB OUTPUT pin-out X01

Acronym		Full name	Connector	Pin	Pin
IRB()_SP<0>	IRB()_SN<0>	8kHz ref. signals	X01	A05	B05
IRB()_SP<1>	IRB()_SN<1>	-"	X01	A06	B06
IRB()_SP<2>	IRB()_SN<2>	-"	X01	A07	B07
IRB()_SP<3>	IRB()_SN<3>	-"	X01	A08	B08
IRB()_SP<4>	IRB()_SN<4>	-"	X01	A09	B09
IRB()_SP<5>	IRB()_SN<5>	-"	X01	A10	B10

() = 0 or 1

Table 40. CGB_0 INPUT pin-out X01

Acronym		Full name	Connector	Pin	Pin
IRB0_SP<0>	IRB0_SN<0>	8kHz ref. signals	X01	A05	B05
IRB0_SP<1>	IRB0_SN<1>	-"	X01	A06	B06
IRB0_SP<2>	IRB0_SN<2>	-"	X01	A07	B07
IRB1_SP<0>	IRB1_SN<0>	-"	X01	A08	B08
IRB1_SP<1>	IRB1_SN<1>	-"	X01	A09	B09
IRB1_SP<2>	IRB1_SN<2>	-"	X01	A10	B10

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Table 41. CGB_1 INPUT pin-out X01

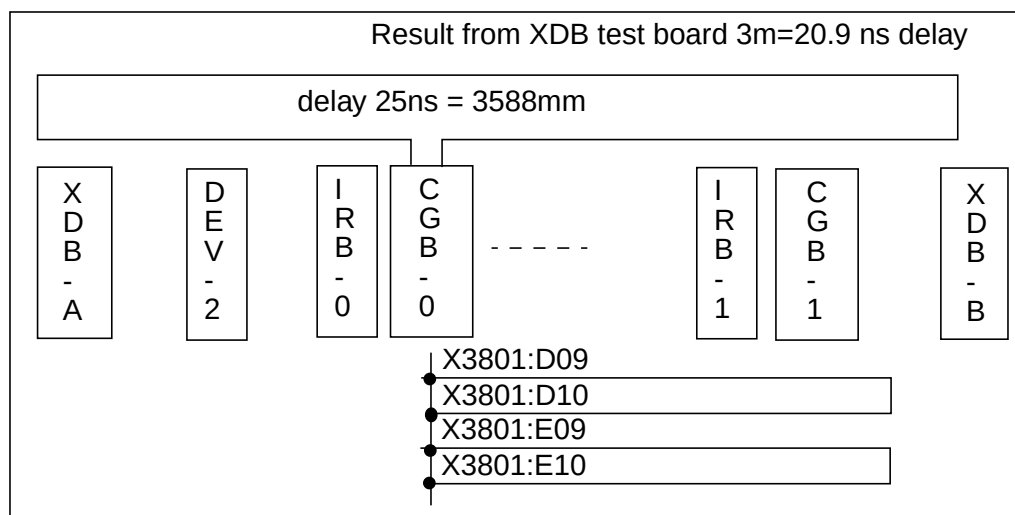
Acronym		Full name	Connector	Pin	Pin
IRB0_SP<3>	IRB0_SN<3>	8kHz ref. signals	X01	A05	B05
IRB0_SP<4>	IRB0_SN<4>	-"	X01	A06	B06
IRB0_SP<5>	IRB0_SN<5>	-"	X01	A07	B07
IRB1_SP<3>	IRB1_SN<3>	-"	X01	A08	B08
IRB1_SP<4>	IRB1_SN<4>	-"	X01	A09	B09
IRB1_SP<5>	IRB1_SN<5>	-"	X01	A10	B10

9.11.3.1 Layout information

LVDS differential pair 100 Ohm.

9.11.4 CGB_0 delay signal

The clock signal from CGB_0 shall be delayed in the backplane (25ns) compared to CGB_1.

Fig.39. CGB delay**Table 42. CGB_0 Delay**

Acronym		Full name	Connector	Pin	Pin
IN_CLK_DLY_P	IN_CLK_DLY_N	Clock delay in	X01	D09	E09
OUT_CLK_DLY_P	OUT_CLK_DLY_N	Clock delay out	X01	D10	E10

9.11.4.1 Layout information

Differential pair 100 Ohm.

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10 SIGNAL DISTRIBUTION (CONNECTORS)

The new five-row Teradyne connector that features two pairs of signals and a ground plane and fits a15mm slot-to-slot pitch shall be used for all boards in GEM.

The SCB-RP board (30mm) consist of mother and daughter board using physical position X02/X05 and X80/X83.

The same is valid for CGB using physical position X38/X41 and X71/X74(16k).

Note !! All CGB connectors are not used in GEM.

10.1 MB, JTAG (SCB-RP)

Connector pins not accessed by the backplane are shadowed (green).

SCB-RP will be used for termination of the JTAG2 bus (backplane).

Table 43. X01_Mother board

ROW	COLUMN				
	A	B	C	D	E
01	SENSE_U	MB_WCZ	GND	JTAG2_TCK	JTAG2_TRST
02	MB_A0	MB_A1	GND	MB_A2	MB_A3
03	MB_A4	MB()_SDA<n>	GND	JTAG2_TDI	JTAG2_TMS
04	MB()_SCL<n>	MB()_3V	GND	JTAG2_TDO	ASP_BYPZ
05	NC	NC	GND	MBM()_3V	MBM()_3V
06	JTAG2_TCK-term	JTAG2_TMS-term	GND	JTAG2_TDI-term	JTAG2_TDO-term
07	MB()_SCL<1>	NC	GND	MB()_SDA<1>	NC
08	MB()_SCL<2>	NC	GND	MB()_SDA<2>	NC
09	MB()_SCL<3>	NC	GND	MB()_SDA<3>	NC
10			GND		

() = A or B

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10.2 ETHERNET SLAVE, RPB-S MASTER/SLAVE (SCB-RP)

Connector pins not used in the backplane are shadowed (green)

Table 44. X10_Mother board

ROW	COLUMN				
	A	B	C	D	E
01	10BaseTA_TXP	10BaseTA_TXN	GND	10BaseTB_TXN	10BaseTB_TXP
02	10BaseTA_RXP	10BaseTA_RXN	GND	10BaseTB_RXN	10BaseTB_RXP
03	1000BaseTA_TXP	1000BaseTA_TXN	GND	1000BaseTB_TXN	1000BaseTB_TXP
04	1000BaseTA_RXP	1000BaseTA_RXN	GND	1000BaseTB_RXN	1000BaseTB_RXP
05	NC	EA_SRE	GND	EB_SRE	AP_0-SP
06	AP_0-S0	AP_0-S1	GND	AP_0-S2	AP_0-S3
07	RPB/M()_TX<1>	RPB/M()_TX<2>	GND	RPB/M()_TX<3>	RPB/M()_TX<4>
08	RPB/M()_RX<1>	RPB/M()_RX<2>	GND	RPB/M()_RX<3>	RPB/M()_RX<4>
09	NC	RPB/MA_TX<n>	GND	RPB/MB_TX<n>	NC
10	NC	RPB/MA_RX<n>	GND	RPB/MB_RX<n>	NC

To solve ethernet with differential and single-ended connection the polarity for 10BASET branch-B is changed (see yellow signals)

NC pins can be used for test signals.

10.3 ADDRESS PLUGS, JTAG1, PBIST (SCB-RP)

Table 45. X11_Mother board

ROW	COLUMN				
	A	B	C	D	E
01	AP_1-S0	AP_1-S1	GND	AP_1-S2	AP_1-S3
02	AP_1-SP	AP_3-S0	GND	AP_3-S1	AP_3-S2
03	AP_3-S3	AP_3-SP	GND	BADR-S0	BADR-S1
04	BADR-S2	BADR-S3	GND	BADR-S4	BADR-SP
05	MTC_TRSTZ	JTAG1_TCK	GND	JTAG1_TDI	MTC_TDO
06	JTAG1_TRSTZ	JTAG1_TMS	GND	JTAG1_TDO	FWZ
07	TAP_HRSTZ	TRG	GND	FWPEZ	NC
08	P3V	PGND	GND	TMPZ0	TMPZ1
09	MTC_TCK	V24_TX	GND	V24_RX	NC
10	SENSE_L	MTC_TMS	GND	MTC_TDI	Vcc_mon

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10.4 ETHERNET MASTER (SCB-RP))

Table 46. X06_Daughter board

ROW	COLUMN				
	A	B	C	D	E
01	10BaseT_TXP_0	10BaseT_TXN_0	GND	1000BaseT_TXP_0	1000BaseT_TXN_0
02	10BaseT_RXP_0	10BaseT_RXN_0	GND	1000BaseT_RXP_0	1000BaseT_RXN_0
03	10BaseT_TXP_1	10BaseT_TXN_1	GND	1000BaseT_TXP_1	1000BaseT_TXN_1
04	10BaseT_RXP_1	10BaseT_RXN_1	GND	1000BaseT_RXP_1	1000BaseT_RXN_1
05	10BaseT_TXP_2	10BaseT_TXN_2	GND	1000BaseT_TXP_2	1000BaseT_TXN_2
06	10BaseT_RXP_2	10BaseT_RXN_2	GND	1000BaseT_RXP_2	1000BaseT_RXN_2
07	10BaseT_TXP_3	10BaseT_TXN_3	GND	1000BaseT_TXP_3	1000BaseT_TXN_3
08	10BaseT_RXP_3	10BaseT_RXN_3	GND	1000BaseT_RXP_3	1000BaseT_RXN_3
09	10BaseT_TXP_4	10BaseT_TXN_4	GND	1000BaseT_TXP_4	1000BaseT_TXN_4
10	10BaseT_RXP_4	10BaseT_RXN_4	GND	1000BaseT_RXP_4	1000BaseT_RXN_4

Table 47. X07_Daughter board

ROW	COLUMN				
	A	B	C	D	E
01	10BaseT_TXP_5	10BaseT_TXN_5	GND	1000BaseT_TXP_5	1000BaseT_TXN_5
02	10BaseT_RXP_5	10BaseT_RXN_5	GND	1000BaseT_RXP_5	1000BaseT_RXN_5
03	10BaseT_TXP_6	10BaseT_TXN_6	GND	1000BaseT_TXP_6	1000BaseT_TXN_6
04	10BaseT_RXP_6	10BaseT_RXN_6	GND	1000BaseT_RXP_6	1000BaseT_RXN_6
05	10BaseT_TXP_7	10BaseT_TXN_7	GND	1000BaseT_TXP_7	1000BaseT_TXN_7
06	10BaseT_RXP_7	10BaseT_RXN_7	GND	1000BaseT_RXP_7	1000BaseT_RXN_7
07	10BaseT_TXP_8	10BaseT_TXN_8	GND	1000BaseT_TXP_8	1000BaseT_TXN_8
08	10BaseT_RXP_8	10BaseT_RXN_8	GND	1000BaseT_RXP_8	1000BaseT_RXN_8
09	10BaseT_TXP_9	10BaseT_TXN_9	GND	1000BaseT_TXP_9	1000BaseT_TXN_9
10	10BaseT_RXP_9	10BaseT_RXN_9	GND	1000BaseT_RXP_9	1000BaseT_RXN_9

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Table 48. X08_Daughter board

ROW	COLUMN				
	A	B	C	D	E
01	10BaseT_TXP_10	10BaseT_TXN_10	GND	1000BaseT_TXP_10	1000BaseT_TXN_10
02	10BaseT_RXP_10	10BaseT_RXN_10	GND	1000BaseT_RXP_10	1000BaseT_RXN_10
03	10BaseT_TXP_11	10BaseT_TXN_11	GND	1000BaseT_TXP_11	1000BaseT_TXN_11
04	10BaseT_RXP_11	10BaseT_RXN_11	GND	1000BaseT_RXP_11	1000BaseT_RXN_11
05	10BaseT_TXP_12	10BaseT_TXN_12	GND	1000BaseT_TXP_12	1000BaseT_TXN_12
06	10BaseT_RXP_12	10BaseT_RXN_12	GND	1000BaseT_RXP_12	1000BaseT_RXN_12
07	10BaseT_TXP_13	10BaseT_TXN_13	GND	1000BaseT_TXP_13	1000BaseT_TXN_13
08	10BaseT_RXP_13	10BaseT_RXN_13	GND	1000BaseT_RXP_13	1000BaseT_RXN_13
09	10BaseT_TXP_14	10BaseT_TXN_14	GND	1000BaseT_TXP_14	1000BaseT_TXN_14
10	10BaseT_RXP_14	10BaseT_RXN_14	GND	1000BaseT_RXP_14	1000BaseT_RXN_14

Table 49. X09_Daughter board

ROW	COLUMN				
	A	B	C	D	E
01	10BaseT_TXP_15	10BaseT_TXN_15	GND	1000BaseT_TXP_15	1000BaseT_TXN_15
02	10BaseT_RXP_15	10BaseT_RXN_15	GND	1000BaseT_RXP_15	1000BaseT_RXN_15
03	10BaseT_TXP_16	10BaseT_TXN_16	GND	1000BaseT_TXP_16	1000BaseT_TXN_16
04	10BaseT_RXP_16	10BaseT_RXN_16	GND	1000BaseT_RXP_16	1000BaseT_RXN_16
05	10BaseT_TXP_17	10BaseT_TXN_17	GND	1000BaseT_TXP_17	1000BaseT_TXN_17
06	10BaseT_RXP_17	10BaseT_RXN_17	GND	1000BaseT_RXP_17	1000BaseT_RXN_17
07	10BaseT_TXP_18	10BaseT_TXN_18	GND	1000BaseT_TXP_18	1000BaseT_TXN_18
08	10BaseT_RXP_18	10BaseT_RXN_18	GND	1000BaseT_RXP_18	1000BaseT_RXN_18
09	10BaseT_TXP_19	10BaseT_TXN_19	GND	1000BaseT_TXP_19	1000BaseT_TXN_19
10	10BaseT_RXP_19	10BaseT_RXN_19	GND	1000BaseT_RXP_19	1000BaseT_RXN_19

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Table 50. X10_Daughter board

ROW	COLUMN				
	A	B	C	D	E
01	10BaseT_TXP_20	10BaseT_TXN_20	GND	1000BaseT_TXP_20	1000BaseT_TXN_20
02	10BaseT_RXP_20	10BaseT_RXN_20	GND	1000BaseT_RXP_20	1000BaseT_RXN_20
03	10BaseT_TXP_21	10BaseT_TXN_21	GND	1000BaseT_TXP_21	1000BaseT_TXN_21
04	10BaseT_RXP_21	10BaseT_RXN_21	GND	1000BaseT_RXP_21	1000BaseT_RXN_21
05	10BaseT_TXP_22	10BaseT_TXN_22	GND	1000BaseT_TXP_22	1000BaseT_TXN_22
06	10BaseT_RXP_22	10BaseT_RXN_22	GND	1000BaseT_RXP_22	1000BaseT_RXN_22
07	10BaseT_TXP_23	10BaseT_TXN_23	GND	1000BaseT_TXP_23	1000BaseT_TXN_23
08	10BaseT_RXP_23	10BaseT_RXN_23	GND	1000BaseT_RXP_23	1000BaseT_RXN_23
09	10BaseT_TXP_24	10BaseT_TXN_24	GND	1000BaseT_TXP_24	1000BaseT_TXN_24
10	10BaseT_RXP_24	10BaseT_RXN_24	GND	1000BaseT_RXP_24	1000BaseT_RXN_24

Table 51. X11_Daughter board

ROW	COLUMN				
	A	B	C	D	E
01	10BaseT_TXP_25	10BaseT_TXN_25	GND	1000BaseT_TXP_25	1000BaseT_TXN_25
02	10BaseT_RXP_25	10BaseT_RXN_25	GND	1000BaseT_RXP_25	1000BaseT_RXN_25
03	E_SRE_1	E_SRE_2	GND	E_SRE_3	E_SRE_4
04	E_SRE_5	E_SRE_6	GND	E_SRE_7	E_SRE_8
05	E_SRE_9	E_SRE_10	GND	E_SRE_11	E_SRE_12
06	E_SRE_13	E_SRE_14	GND	E_SRE_15	E_SRE_16
07	E_SRE_17	E_SRE_18	GND	E_SRE_19	E_SRE_20
08	E_SRE_21	E_SRE_22	GND	E_SRE_23	E_SRE_24
09	E_SRE_25	E_SRE_0	GND		
10			GND		

The E_SRE pins are only used in combination with old SCB-RP boards and adapters towards GEM. E_SRE_0 was place last due to an error.

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				File	

10.5 MB, INTERNAL CLOCK/SYNC (XDB AND XNB)

Connector pins not used in the backplane are shadowed (green).

Table 52. X01 position XDB, XNB

ROW	COLUMN				
	A	B	C	D	E
01	SENSE_U	MB_WC	GND	JTAG2_TCK	JTAG2_TRST
02	MB_A0	MB_A1	GND	MB_A2	MB_A3
03	MB_A4	MBAorB_SDA<n>	GND	JTAG2_TDI	JTAG2_TMS
04	MBAorB_SCL<n>	MBAorB_3V	GND	JTAG2_TDO	ASP_BYPZ
05	NC	NC	GND	CX()_CP<0or1, 2or3>	CX()_CN<0or1, 2or3>
06	NC	NC	GND	CX()_SP<0or1, 2or3>	CX()_SN<0or1, 2or3>
07	NC	NC	GND	XC()_SP<0or1, 2or3>	XC()_SN<0or1, 2or3>
08	NC	NC	GND	CX()_CP<0or1, 2or3>	CX()_CN<0or1, 2or3>
09	NC	NC	GND	CX()_SP<0or1, 2or3>	CX()_SN<0or1, 2or3>
10	NC	NC	GND	XC()_SP<0or1, 2or3>	XC()_SN<0or1, 2or3>

() = 0 or 1 <0 and 1> = XDB <2 and 3> = XNB

10.6 MB, REF.CLOCKS OUT IRB (TO CGB)

Table 53. X01 position IRB

ROW	COLUMN				
	A	B	C	D	E
01	SENSE_U	MB_WC	GND	JTAG2_TCK	JTAG2_TRST
02	MB_A0	MB_A1	GND	MB_A2	MB_A3
03	MB_A4	MB()_SDA<n>	GND	JTAG2_TDI	JTAG2_TMS
04	MB()_SCL<n>	MB()_3V	GND	JTAG2_TDO	ASP_BYPZ
05	IRB():SP<0>	IRB():SN<0>	GND	NC	NC
06	IRB():SP<1>	IRB():SN<1>	GND	NC	NC
07	IRB():SP<2>	IRB():SN<2>	GND	NC	NC
08	IRB():SP<3>	IRB():SN<3>	GND	NC	NC
09	IRB():SP<4>	IRB():SN<4>	GND	NC	NC
10	IRB():SP<5>	IRB():SN<5>	GND	NC	NC

MB() = A or B () = 0 or 1 (IRB)

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10.7 MB, CGB (FROM IRB)

Connector pins not used in the backplane are shadowed (green).

Table 54. X01 position CGB

ROW	COLUMN				
	A	B	C	D	E
01	SENSE_U	MB_WC	GND	JTAG2_TCK	JTAG2_TRST
02	MB_A0	MB_A1	GND	MB_A2	MB_A3
03	MB_A4	MB()_SDA<n>	GND	JTAG2_TDI	JTAG2_TMS
04	MB()_SCL<n>	MB()_3V	GND	JTAG2_TDO	ASP_BYPZ
05	IRB0_SP<0, 3>	IRB0_SN<0, 3>	GND	NC	NC
06	IRB0_SP<1, 4>	IRB0_SN<1, 4>	GND	NC	NC
07	IRB0_SP<2, 5>	IRB0_SN<2, 5>	GND	NC	NC
08	IRB1_SP<0, 3>	IRB1_SN<0, 3>	GND	NC	NC
09	IRB1_SP<1, 4>	IRB1_SN<1, 4>	GND	CLK_DLY_INP_P	CLK_DLY_INP_N
10	IRB1_SP<2, 5>	IRB1_SN<2, 5>	GND	CLK_DLY_OUT_P	CLK_DLY_OUT_N

IRB <0, 1 and 2> = CGB_0 <3,4 and 5> = CGB_1

MB() = A or B

10.8 MB, OTHERS

Table 55. X01 position Others

ROW	COLUMN				
	A	B	C	D	E
01	SENSE_U	MB_WC	GND	JTAG2_TCK	JTAG2_TRST
02	MB_A0	MB_A1	GND	MB_A2	MB_A3
03	MB_A4	MB()_SDA<n>	GND	JTAG2_TDI	JTAG2_TMS
04	MB()_SCL<n>	MB()_3V	GND	JTAG2_TDO	ASP_BYPZ
05	NC	NC	GND	NC	NC
06	NC	NC	GND	NC	NC
07	NC	NC	GND	NC	NC
08	NC	NC	GND	NC	NC
09	NC	NC	GND	NC	NC
10	NC	NC	GND	NC	NC

MB() = A or B

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10.9 INTERNAL/EXTERNAL CLOCK/SYNC OUT (CGB)

Table 56. X02 position CGB

ROW	COLUMN				
	A	B	C	D	E
01	CX()_CP<0>	CX()_CN<0>	GND	CX()_CP<1>	CX()_CN<1>
02	CX()_SP<0>	CX()_SN<0>	GND	CX()_SP<1>	CX()_SN<1>
03	XC()_SP<0>	XC()_SN<0>	GND	XC()_SP<1>	XC()_SN<1>
04	CX()_CP<2>	CX()_CN<2>	GND	CX()_CP<3>	CX()_CN<3>
05	CX()_SP<2>	CX()_SN<2>	GND	CX()_SP<3>	CX()_SN<3>
06	XC()_SP<2>	XC()_SN<2>	GND	XC()_SP<3>	XC()_SN<3>
07	CX()_CP_0<7>	CX()_CN_0<7>	GND	CX()_CP_0<6>	CX()_CN_0<6>
08	CX()_SP_0<7>	CX()_SN_0<7>	GND	CX()_SP_0<6>	CX()_SN_0<6>
09	XC()_SP_0<7>	XC()_SN_0<7>	GND	XC()_SP_0<6>	XC()_SN_0<6>
10	CX()_CP_0<5>	CX()_CN_0<5>	GND	CX()_CP_0<4>	CX()_CN_0<4>

() = 0 or 1 (CGB)

10.10 DL34 AND ET155 PROTECTION SWITCH INTERFACE (DEV)

Connector pins not used in the backplane are shadowed (green).

Table 57. X04 DEvIce positions (CDB see next table)

ROW	COLUMN				
	A	B	C	D	E
01	XLB_DP<n>	XLB_DN<n>	GND	NC	NC
02	XLB_CP<n>	XLB_CN<n>	GND	NC	NC
03	LXB_DP<n>	LXB_DN<n>	GND	NC	NC
04	NC	NC	GND	NC	NC
05	TX_DP_PSI	TX_DN_PSI	GND	RX_DP_PSI	RX_DN_PSI
06	TX_CP_PSI	TX_CN_PSI	GND	RX_CP_PSI	RX_CN_PSI
07	NC	NC	GND	NC	NC
08	XLA_DP<n>	XLA_DN<n>	GND	NC	NC
09	XLA_CP<n>	XLA_CN<n>	GND	NC	NC
10	LXA_DP<n>	LXA_DN<n>	GND	NC	NC

n = 0-21

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		2001-12-13		D	
				File	

Table 58. X04 CDB positions

ROW	COLUMN				
	A	B	C	D	E
01	XLB_DP<n>	XLB_DN<n>	GND	CX()_CP_0<7>	CX()_CN_0<7>
02	XLB_CP<n>	XLB_CN<n>	GND	CX()_SP_0<7>	CX()_SN_0<7>
03	LXB_DP<n>	LXB_DN<n>	GND	XC()_SP_0<7>	XC()_SN_0<7>
04	NC	NC	GND	NC	NC
05	TX_DP_PSI	TX_DN_PSI	GND	RX_DP_PSI	RX_DN_PSI
06	TX_CP_PSI	TX_CN_PSI	GND	RX_CP_PSI	RX_CN_PSI
07	NC	NC	GND	NC	NC
08	XLA_DP<n>	XLA_DN<n>	GND	CX()_CP_0<6>	CX()_CN_0<6>
09	XLA_CP<n>	XLA_CN<n>	GND	CX()_SP_0<6>	CX()_SN_0<6>
10	LXA_DP<n>	LXA_DN<n>	GND	XC()_SP_0<6>	XC()_SN_0<6>

() = 0 or 1 (from CGB)

n = 0 - 21

10.11 DL34 OUT (XDB)

Table 59. X03 XDB(A or B) positions

ROW	COLUMN				
	A	B	C	D	E
01	XL()_DP<0>	XL()_DN<0>	GND	XL()_DP<1>	XL()_DN<1>
02	XL()_CP<0>	XL()_CN<0>	GND	XL()_CP<1>	XL()_CN<1>
03	LX()_DP<0>	LX()_DN<0>	GND	LX()_DP<1>	LX()_DN<1>
04	XL()_DP<2>	XL()_DN<2>	GND	XL()_DP<3>	XL()_DN<3>
05	XL()_CP<2>	XL()_CN<2>	GND	XL()_CP<3>	XL()_CN<3>
06	LX()_DP<2>	LX()_DN<2>	GND	LX()_DP<3>	LX()_DN<3>
07	XL()_DP<4>	XL()_DN<4>	GND	XL()_DP<5>	XL()_DN<5>
08	XL()_CP<4>	XL()_CN<4>	GND	XL()_CP<5>	XL()_CN<5>
09	LX()_DP<4>	LX()_DN<4>	GND	LX()_DP<5>	LX()_DN<5>
10	NC	NC	GND	NC	NC

() = A or B

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Connector pins not used in the backplane are shadowed (green).

Table 60. X04 XDB position

ROW	COLUMN				
	A	B	C	D	E
01	XL()_DP<6>	XL()_DN<6>	GND	XL()_DP<7>	XL()_DN<7>
02	XL()_CP<6>	XL()_CN<6>	GND	XL()_CP<7>	XL()_CN<7>
03	LX()_DP<6>	LX()_DN<6>	GND	LX()_DP<7>	LX()_DN<7>
04	XL()_DP<8>	XL()_DN<8>	GND	XL()_DP<9>	XL()_DN<9>
05	XL()_CP<8>	XL()_CN<8>	GND	XL()_CP<9>	XL()_CN<9>
06	LX()_DP<8>	LX()_DN<8>	GND	LX()_DP<9>	LX()_DN<9>
07	XL()_DP<10>	XL()_DN<10>	GND	XL()_DP<11>	XL()_DN<11>
08	XL()_CP<10>	XL()_CN<10>	GND	XL()_CP<11>	XL()_CN<11>
09	LX()_DP<10>	LX()_DN<10>	GND	LX()_DP<11>	LX()_DN<11>
10	NC	NC	GND	NC	NC

() = A or B

Table 61. X05 XDB

ROW	COLUMN				
	A	B	C	D	E
01	XL()_DP<12>	XL()_DN<12>	GND	XL()_DP<13>	XL()_DN<13>
02	XL()_CP<12>	XL()_CN<12>	GND	XL()_CP<13>	XL()_CN<13>
03	LX()_DP<12>	LX()_DN<12>	GND	LX()_DP<13>	LX()_DN<13>
04	XL()_DP<14>	XL()_DN<14>	GND	XL()_DP<15>	XL()_DN<15>
05	XL()_CP<14>	XL()_CN<14>	GND	XL()_CP<15>	XL()_CN<15>
06	LX()_DP<14>	LX()_DN<14>	GND	LX()_DP<15>	LX()_DN<15>
07	XL()_DP<16>	XL()_DN<16>	GND	XL()_DP<17>	XL()_DN<17>
08	XL()_CP<16>	XL()_CN<16>	GND	XL()_CP<17>	XL()_CN<17>
09	LX()_DP<16>	LX()_DN<16>	GND	LX()_DP<17>	LX()_DN<17>
10	NC	NC	GND	NC	NC

() = A or B

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		2001-12-13		D	File

Connector pins not used in the backplane are shadowed (green).

Table 62. X06 XDB

ROW	COLUMN				
	A	B	C	D	E
01	XL()_DP<18>	XL()_DN<18>	GND	XL()_DP<19>	XL()_DN<19>
02	XL()_CP<18>	XL()_CN<18>	GND	XL()_CP<19>	XL()_CN<19>
03	LX()_DP<18>	LX()_DN<18>	GND	LX()_DP<19>	LX()_DN<19>
04	XL()_DP<20>	XL()_DN<20>	GND	XL()_DP<21>	XL()_DN<21>
05	XL()_CP<20>	XL()_CN<20>	GND	XL()_CP<21>	XL()_CN<21>
06	LX()_DP<20>	LX()_DN<20>	GND	LX()_DP<21>	LX()_DN<21>
07	NC	NC	GND	NC	NC
08	NC	NC	GND	NC	NC
09	NC	NC	GND	NC	NC
10	NC	NC	GND	NC	NC

() = A or B

10.12 EXT. CLOCK/SYNC OUT CGB (TO CDB)

Table 63. X06 CGB

ROW	COLUMN				
	A	B	C	D	E
01	CX()_SP_0<5>	CX()_SN_0<5>	GND	CX()_SP_0<4>	CX()_SN_0<4>
02	XC()_SP_0<5>	XC()_SN_0<5>	GND	XC()_SP_0<4>	XC()_SN_0<4>
03	CX()_CP_0<3>	CX()_CN_0<3>	GND	CX()_CP_0<2>	CX()_CN_0<2>
04	CX()_SP_0<3>	CX()_SN_0<3>	GND	CX()_SP_0<2>	CX()_SN_0<2>
05	XC()_SP_0<3>	XC()_SN_0<3>	GND	XC()_SP_0<2>	XC()_SN_0<2>
06	CX()_CP_0<1>	CX()_CN_0<1>	GND	CX()_CP_0<0>	CX()_CN_0<0>
07	CX()_SP_0<1>	CX()_SN_0<1>	GND	CX()_SP_0<0>	CX()_SN_0<0>
08	XC()_SP_0<1>	XC()_SN_0<1>	GND	XC()_SP_0<0>	XC()_SN_0<0>
09	CX()_CP_1<7>	CX()_CN_1<7>	GND	CX()_CP_1<6>	CX()_CN_1<6>
10	CX()_SP_1<7>	CX()_SN_1<7>	GND	CX()_SP_1<6>	CX()_SN_1<6>

() = 0 or 1

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10.13 EXT. CLOCK/SYNC OUT CGB (TO CDB)

Table 64. X06 CGB daughter position

ROW	COLUMN				
	A	B	C	D	E
01	XC()_SP_1<7>	XC()_SN_1<7>	GND	XC()_SP_1<6>	XC()_SN_1<6>
02	CX()_CP_1<5>	CX()_CN_1<5>	GND	CX()_CP_1<4>	CX()_CN_1<4>
03	CX()_SP_1<5>	CX()_SN_1<5>	GND	CX()_SP_1<4>	CX()_SN_1<4>
04	XC()_SP_1<5>	XC()_SN_1<5>	GND	XC()_SP_1<4>	XC()_SN_1<4>
05	CX()_CP_1<3>	CX()_CN_1<3>	GND	CX()_CP_1<2>	CX()_CN_1<2>
06	CX()_SP_1<3>	CX()_SN_1<3>	GND	CX()_SP_1<2>	CX()_SN_1<2>
07	XC()_SP_1<3>	XC()_SN_1<3>	GND	XC()_SP_1<2>	XC()_SN_1<2>
08	CX()_CP_1<1>	CX()_CN_1<1>	GND	CX()_CP_1<0>	CX()_CN_1<0>
09	CX()_SP_1<1>	CX()_SN_1<1>	GND	CX()_SP_1<0>	CX()_SN_1<0>
10	XC()_SP_1<1>	XC()_SN_1<1>	GND	XC()_SP_1<0>	XC()_SN_1<0>

() = 0 or 1

10.14 CLOCK/SYNC DISTR. CDB (FROM CGB)

Table 65. X07 CDB

ROW	COLUMN				
	A	B	C	D	E
01	CX()_CP()<5>	CX()_CN()<5>	GND	CX()_CP()<4>	CX()_CN()<4>
02	CX()_SP()<5>	CX()_SN()<5>	GND	CX()_SP()<4>	CX()_SN()<4>
03	XC()_SP()<5>	XC()_SN()<5>	GND	XC()_SP()<4>	XC()_SN()<4>
04	CX()_CP()<3>	CX()_CN()<3>	GND	CX()_CP()<2>	CX()_CN()<2>
05	CX()_SP()<3>	CX()_SN()<3>	GND	CX()_SP()<2>	CX()_SN()<2>
06	XC()_SP()<3>	XC()_SN()<3>	GND	XC()_SP()<2>	XC()_SN()<2>
07	CX()_CP()<1>	CX()_CN()<1>	GND	CX()_CP()<0>	CX()_CN()<0>
08	CX()_SP()<1>	CX()_SN()<1>	GND	CX()_SP()<0>	CX()_SN()<0>
09	XC()_SP()<1>	XC()_SN()<1>	GND	XC()_SP()<0>	XC()_SN()<0>
10	GND	GND	GND	GND	GND

() = 0 or 1

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10.15 ETHERNET AND RPB-S (OTHERS)

Connector pins not used in the backplane are shadowed (green).

Table 66. X10 DEVICE BOARDS

ROW	COLUMN				
	A	B	C	D	E
01	10BaseTA_TXP	10BaseTA_TXN	GND	10BaseTB_TXN	10BaseTB_TXP
02	10BaseTA_RXP	10BaseTA_RXN	GND	10BaseTB_RXN	10BaseTB_RXP
03	1000BaseTA_TXP	1000BaseTA_TXN	GND	1000BaseTB_TXN	1000BaseTB_TXP
04	1000BaseTA_RXP	1000BaseTA_RXN	GND	1000BaseTB_RXN	1000BaseTB_RXP
05	NC (CLK_DISZ)	EA_SRE	GND	EB_SRE	AP_0-SP
06	AP_0-S0	AP_0-S1	GND	AP_0-S2	AP_0-S3
07	NC	NC	GND	NC	NC
08	NC	NC	GND	NC	NC
09	NC (CLK3_TST)	RPB/MA_TX<n>	GND	RPB/MB_TX<n>	NC (TC_ENZ)
10	NC (CLK2_TST)	RPB/MA_RX<n>	GND	RPB/MB_RX<n>	NC (CLK1_TST)

To solve ethernet with differential and single-ended connection the polarity for 10BASET branch-B is changed (see yellow signals)

NC pins can be used for board test (production). On XDB the on board oscillator outputs are available. CLK_DISZ = disable system clock TC_ENZ = enable clock output for test.

10.16 JTAG, PBIST AND ADDRESS (OTHERS)

Table 67. X11 Others

ROW	COLUMN				
	A	B	C	D	E
01	AP_1-S0	AP_1-S1	GND	AP_1-S2	AP_1-S3
02	AP_1-SP	AP_3-S0	GND	AP_3-S1	AP_3-S2
03	AP_3-S3	AP_3-SP	GND	BADR-S0	BADR-S1
04	BADR-S2	BADR-S3	GND	BADR-S4	BADR-SP
05	MTC_TRSTZ	JTAG1_TCK	GND	JTAG1_TDI	MTC_TDO
06	JTAG1_TRSTZ	JTAG1_TMS	GND	JTAG1_TDO	FWZ
07	TAP_HRSTZ	TRG	GND	FWPEZ	NC
08	P3V	PGND	GND	TMPZ0	TMPZ1
09	MTC_TCK	V24_TX	GND	V24_RX	NC
10	SENSE_L	MTC_TMS	GND	MTC_TDI	Vcc_mon

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				File	

11ADDRESS INFORMATION

11.1BOARD ADDRESS

Table 68. Board address

Acronym			BADR_P	BADR_4	BADR_3	BADR_2	BADR_1	BADR_0
Physical_Pos	Board_ADR	DEV	X11:E04	X11:D04	X11:B04	X11:A04	X11:E03	X11:D03
X02	0	-	1	0	0	0	0	0
X08	1	0	0	0	0	0	0	1
X11	2	1	0	0	0	0	1	0
X14	3	2	1	0	0	0	1	1
X17	4	3	0	0	0	1	0	0
X20	5	4	1	0	0	1	0	1
X23	6	5	1	0	0	1	1	0
X26	7	6	0	0	0	1	1	1
X29	8	7	0	0	1	0	0	0
X32	9	8	1	0	1	0	0	1
X35	10	9	1	0	1	0	1	0
X38	11	10	0	0	1	0	1	1
X41	12	11	1	0	1	1	0	0
X44	13	12	0	0	1	1	0	1
X47	14	13	0	0	1	1	1	0
X50	15	14	1	0	1	1	1	1
X53	16	15	0	1	0	0	0	0
X56	17	16	1	1	0	0	0	1
X59	18	17	1	1	0	0	1	0
X62	19	18	0	1	0	0	1	1
X65	20	19	1	1	0	1	0	0
X68	21	20	0	1	0	1	0	1
X71	22	21	0	1	0	1	1	0
X74	23	22	1	1	0	1	1	1
X77	24	23	1	1	1	0	0	0
X80	25		0	1	1	0	0	1

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12 DESIGN METHODOLOGY

12.1 DESIGN FLOW

The GEM will be developed by using the PBA/PCB Design Process described in UAB/X/M home page (uabweb.uab.ericsson.se/inside/units/x/m/)

12.2 CAD & TOOLS

The main tool to be used to design, implement and verify the GEM are the following:

- SS2 (Support System 2 from ETX) Concept for schematic entry, Spectra Quest as constraints editor and Allegro for physical design and manual routing.
- Spectra for auto routing
- Spectra Quest/Signoise for analysis
- UCAM to check the physical implementation against the Ericsson productibility requirements

12.3 DESIGN RULES

The design of the GEM will be carried out in accordance with rules stated in the BX hardware design manual.